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RADC ltr, 22 Jan 1980

RADC-TR-75-50
Final Technical Report
March 1975

RELIABILITY STUDY OF BEAM LEAD SEALED JUNCTION DEVICES

Hughes Aircraft Co.

Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-75-50	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): RELIABILITY STUDY OF BEAM LEAD SEALED JUNCTION DEVICES	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report April 1973 - July 1974
	6. PERFORMING ORG. REPORT NUMBER: FR 74-10-772
7. AUTHOR(s): J. J. Mazenko	8. CONTRACT OR GRANT NUMBER(s): F30602-73-C-0204
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Hughes Aircraft Company, Fullerton CA 92634	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: J. O. 55190640
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center/RBRP, Griffiss AFB NY 13441	12. REPORT DATE: March 1975
	13. NUMBER OF PAGES: 122
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Distribution limited to U.S. Gov't agencies only; test and evaluation; March 1975. Other requests for this document must be referred to RADC/RBRP, Griffiss AFB NY 13441.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project engineer:
John J. Bart/RBRP
AC 315 330-2306

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Beam Lead Device
Integrated Circuits

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Over 4000 beam lead sealed junction devices, of nine different types, both linear and digital and from four different manufacturers, were physically and electrically characterized. The devices were then sealed (in hermetic and nonhermetic packages) and were environmentally stressed under both operating and nonoperating conditions. Performance was determined and failures categorized according to type, class, complexity, manufacturer, package, and screen.

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PREFACE

This is the final report of a 15-month study of the reliability of beam lead sealed junction devices. This study was conducted by the Technical Services Group Office of Hughes' Ground Systems Group, Fullerton, California, under Contract F30602-73-C-0204.

The study was conducted under the direction of J.J. Mazenko of the Technical Support Laboratory. This laboratory consists of several interrelated technology departments including Microelectronics, and Components and Materials. The Microelectronics Department was responsible for the overall management of the study and for the fabrication and assembly of the test modules. Electrical testing, screening, failure analysis and module encapsulation were supported by the Components and Materials Department. The detailed thermal mapping analysis was performed by the Environmental Engineering Department. Data Analysis was performed by the Systems Effectiveness Department of the Ground Systems Group.

This technical report has been reviewed and approved for publication.

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CONTENTS

EVALUATION MEMORANDUM

Reliability Study of Beam Lead Sealed Junction Devices

The intent of this program was the generation of reliability information on beam lead sealed junction (BLSJ) devices applicable to their use for military electronic systems. This involved both device limitations and screening/qualification test requirements.

The major study conclusions point out limitations in the test devices in several areas. There were some problems associated with manufacturing defects, such as cracked silicon nitride layers, gold plating defects and possibly junction shorts arising from defective barrier layers and subsequent gold-silicon interaction. There were also fundamental materials problems such as gold deplating in moist environments and surface instabilities of linear devices.

Whereas some of these problems can be eliminated by improved process controls, visual inspection techniques and electrical qualification and screening tests, there are still questions concerning the type of chip protection necessary for reliable operation which are unanswered. We are presently studying polymer chip coating layers on contract F30602-74-C-0161 with Westinghouse Research Laboratories. Information from this study will be integrated with information from other industry and government sources to determine proper design guidelines and reliability test procedures.

The results of the Hughes effort has been discussed with a variety of government and industry sources. Our conclusion based on all information is that beam lead devices have not a demonstrated reliability advantage over chip and wire metallized devices at this time. While isolated examples can be found for successful application of this technology, its broad usage for military electronic systems still requires cautious study.

John J. Bart

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SECTION 1
INTRODUCTION AND SUMMARY

1. REVIEW OF PROGRAM CONDUCT AND MAJOR RESULTS

Beam lead integrated circuits from major suppliers were subjected to operational and non-operational screening tests to validate the claims for improved reliability, higher yields, and net cost reductions. The overriding conclusion resulting from the study was that beam lead devices, unless properly screened and packaged, do not satisfy these claims.

Background – In 1972, more and more military contracts were committing to the use of beam lead devices based on the promise of increased reliability and decreased costs. The improved reliability promise was basically a function of eliminating or reducing failures attendant with standard semiconductor chips, such as wire bond failures, ionic contamination, and interconnect corrosion. Through the use of sealed junction beam lead devices, the metallurgy was reportedly less prone to migration or corrosion, the junctions were sealed with silicon nitride which is impervious to sodium ion contamination, and since the beams were integral with the device they would eliminate wire bond failures. The beam lead devices reportedly would effect a cost reduction in the hybrids in which they were used (even though the cost of beam lead devices were significantly higher than that of a similar chip device) because of reduced assembly times where with the beam lead device bonding could be accomplished in a fraction of that of chip and wire bonding.

Further cost reductions at the hybrid level were anticipated because beam lead devices reportedly could be completely AC tested prior to committing it to hybrid assembly, whereas a bare chip device would be AC tested on a sample basis only. The totally AC-tested beam lead device would increase hybrid yields, reduce rework, and effect a hybrid cost reduction. A further reported advantage was that beam lead devices would operate reliably in non-hermetic packages simply by coating them with a polymer. Thus, elimination of the need for hermetic hybrid packages would also add another significant cost reduction.

Review of Objectives – In 1972, when the study was initiated, actual beam lead reliability and use data was very sparse. Beam lead device reliability predictions were based on experimental results from selected devices, (primarily transistors) fabricated with well controlled laboratory processes. Additionally beam lead manufacturers' reliability data sheets were sparse and here also the data available was primarily based only on transistors. There was, as now, no uniform screening standards for beam lead devices.

It was thus necessary for the military to truly assess the capabilities and limitations of beam lead devices. Here, the devices to be studied would be Beam Lead Integrated Circuits which would be purchased from the major beam lead suppliers. These devices would be representative of the product available to all military users.

They would be put through a series of operational and non-operational screening tests in both hermetic and non-hermetic packages. The devices would be both of the digital and the linear class, with each class containing both simple and complex devices. From these screens and stress tests, the device yields and failure modes as a function of device manufacturer, class, complexity, package (hermetic and non-hermetic) and polymer coating (conformally coated or molded) would be assessed. From these data, recommendations would be made

for beam lead device screening procedures prior to their use in hybrids for military systems.

Scope of the Study – The study consisted of two investigations – beam lead reliability analysis and evaluation of the beam bonding integrity – involving 4241 purchased beam lead devices. Initially, 360 of the devices were used to establish the device characteristics. The principal study effort was devoted to determining the device's reliability. Of the 3681 devices required for this effort, 225 were needed for process set-up samples, and 3456 devices were packaged, screened, and tested under a full factorial experimental design with 16 device samples/cell. The resulting study data is therefore significant to a 70% confidence level. This effort represents over 2.5 million device-hours of accumulated tests.

The secondary study, involving 200 devices, was the replacement/rework study. This effort was conducted to determine the reliability of modules subjected to reiterative device replacement and rework.

A review of the results of these efforts is given on the following page.

Peculiar Study Problems – Some of the problems encountered during the study occurred at the program start. Here neither the prime off-the-shelf beam lead IC's proposed, nor their proposed alternates, were available. Thus, the original device matrix had to be reconfigured to accommodate device availability.

No standardization was found from vendor to vendor on the same device type, thus substrate layouts had to be designed and fabricated for each device purchased instead of merely for each device type.

Variations in beam hardness and beams/device required that wobble bonder settings be optimized for each device type.

Establishing the Stress Test Levels – During the proposal phase of the contract, one of the major concerns was that, due to the reportedly low beam lead device failure rates (0.005%/1000 hours), it would require acceleration factors of 10^6 to provide 8 failures from each cell of 16 devices for failure analysis. The screens selected were either pulled from or adapted from MIL-STD-883 to be representative of those screens which could be used for hybrid screening. Stress levels were set to provide a minimum of 1 to 2 devices per cell, but even then there was grave concern that sufficient failures would be generated to provide meaningful yield and failure mode data. However, these fears proved groundless, for as the devices went through the first screen/stress tests the incidence of failure was so high that we immediately began to question the validity of the device assembly and test procedures.

Verifying the Test Results – A failure verification test to verify rejects from the automated test equipment was implemented. This test, which was not part of the original proposal, was done on a bench set-up by an engineer. Any rejects which were possibly caused by assembly or test abnormalities were noted and deleted from further tests. These assembly-and-test-created rejects proved to be insignificant. The beam lead reject rates from the screens/stress tests were truly high. Personal communication between key members of the study team and other people both within and outside the company found that they also had the same problem and same reaction when using beam lead devices.

REVIEW OF STUDY CONCLUSIONS

Reliability Study Conclusions:

- At present, beam lead devices are not cost effective.
- Beam lead devices, even when ploymer coated, may not operate reliably in nonhermetic environments.
- Improperly processed or inadequately screened beam lead devices fail more readily than standard semiconductor devices.
- Beam lead devices have opened up as many new failure modes as they have eliminated.
- There is no standardization among manufacturer in device processing, device configuration, or device screening.
- There are significant measurable differences in the beam lead device material (silicon nitride, platinum, etc.) layers as processed by the different manufacturers.
- Linear devices fail at a much higher rate than digital devices.
- Reliability and failure rate data currently quoted for beam lead devices must be re-evaluated.

Bond Integrity Study Conclusions:

- Devices can be replaced at a given dice site up to 10 times (limit of this experiment) with no loss in device mechanical strength, yield, or reliability.
- Rework of individual beams should be done by rebonding each loose beam individually rather than rewobble bonding the entire device.

SECTION 2
BEAM LEAD RELIABILITY STUDY

Section 2 – Beam Lead Reliability Study

1. APPROACH TO THE EXPERIMENTAL DESIGN

The test was a full factorial design and was selected to provide broad coverage of the beam lead reliability packaging and screening requirements posed for the study. Also, the test design was configured to contain enough samples (3456) for each combination of variables to provide definitive packaging and screening recommendations.

Both the matrix configuration and the cell sample size were chosen to provide maximum data, with a high statistical confidence level.

The variables selected were device group (linear and digital), device complexity (simple and complex), and device package (hermetic and non-hermetic). The hermetic packages were filled with three different atmospheres, and the non-hermetic were of two types, molded and conformal coated. The molded packages were of two types (with and without mold release), and the conformal coated devices utilized two different types of coatings. The test matrix is shown in Table 1.

As is seen from Table 1, sixteen devices per cell were used. (This translates into 3,456 devices being used for the screens and stress tests.)

Here, with a sample size of 16 devices per cell, the study data has a confidence level of 70 percent, whereas, by comparison, if the cell size were decreased to 10 the confidence level would be less than 50 percent.

The variable of device manufacturer (vendor) was not entirely part of the full factorial design. However, the effect of device manufacturer was easily determined because the device selection was done to ensure that (1) one device was available from all four manufacturers, and (2) one manufacturer supplied both simple and complex linear and digital devices. (This is easily seen later in Table 3, Matrix of Beam Lead Devices Actually Used.)

TABLE 1. EXPERIMENTAL TEST DESIGN

TEST CELL MATRIX FOR INDEPENDENT VARIABLES – EXCEPT MANUFACTURERS

Package	Atmosphere Inside Package		Device Group			
			Analog		Digital	
			Simple	Complex	Simple	Complex
Hermetic	N_2		16	16	16	16
	H_2O Vapor		16	16	16	16
	Salt/H_2O		16	16	16	16
Non-Hermetic (Plastic)	Mold Release		16	16	16	16
	No Mold Release		16	16	16	16
	Conformal Coating	Type 1	16	16	16	16
		Type 2	16	16	16	16

Section 2 – Beam Lead Reliability Study
Subsection A – Device Selection and Characterization

1. SELECTION OF DEVICES FOR THE STUDY

Nine beam lead devices were originally selected on the basis of class (linear or digital) and complexity to represent each of the four manufacturers under consideration. Of these nine, only three were available for testing, and alternate devices were procured as replacements.

The devices proposed for the program were selected from the catalogs of the four major suppliers of beam lead devices in late 1972. The device selection was restricted to those manufacturers which used the Bell Laboratories metallurgy because it was felt that this type of construction most probably would provide a major share of devices to the military market in the forseeable future.

Selection Criteria – Two basic classes of devices were chosen: linear and digital. A simple and a complex device was selected from within each category. Table 2 opposite identifies the specific devices selected by category, complexity, and manufacturer, coded W, X, Y and Z.

Devices were selected to ensure that at least one device would be available from all four manufacturers and that all four devices would be available from at least one manufacturer. This was to provide an evaluation of process variations between manufacturers on the same device as well as process variations within one manufacturing operation on four different devices.

Device Availability – As stated above, the devices proposed for the study were representative of devices available in the marketplace in late 1972. As shown in Table 2, nine devices were originally selected as prime candidates. Even though "off-the-shelf" availability was one criterion for selection of these devices, it was recognized early that procurement could be a problem so alternate devices were established as a precaution. Subsequently, only three of the nine manufacturers' types originally specified were available when ordered, and only in two instances were the first alternates available. When it was apparent that the late deliveries of devices would severely impact the program, the device matrix was reconfigured to utilize devices that the manufacturers recommended as immediately available. The devices which were ultimately used for the study are shown in Table 3. The best device delivery was 4 weeks while the worst delivery was never established (the purchase order was cancelled after 40 weeks).

TABLE 2. BEAM LEAD DEVICES PROPOSED FOR EVALUATION

Device	Function	Vendor W	X	Y	Z
Linear Group					
Simple 741	Operational Amplifier	X	X	X	X
Complex 1596	Balanced Modulator-Demodulator	X			
(Complex 710)*	(Voltage Comparator)				
Digital Group					
Simple 5476	Dual J-K Flip Flop	X			X
(Simple 5400)*	(Quad 2 Input Nand Gate)				
Complex 5490	Decade Counter	X	X		
(Complex 5493)*	(4-Bit Binary Counter)				
Approximate Product Line Availability					
Linear Devices		4	6	8	3
Digital Devices		22	50		32
Total		26	56	8	35

*Alternate Device

TABLE 3. MATRIX OF BEAM LEAD DEVICES ACTUALLY USED

Device	Vendor W	X	Y	Z
Linear Group				
Simple μA 741	X	[RM 101 BL]	X	X
Complex MC 1596	–	–		–
(Complex MC 710)	(MC 710)	–	–	–
Digital Group				
Simple 5476	–	–		[5410]
(Simple 5400)	(5400)	–	–	–
Complex 5490	–	–	–	–
(Complex 5493)	[5473]	[RF 100 BL]	–	–

Legend

( ) – Alternate Device Originally Proposed
[ ] – Closest Available Alternate
X – Originally Proposed

2. CHARACTERIZING THE DEVICES ACCORDING TO ELECTRICAL PARAMETERS

The first characterization task conducted on the purchased beam lead devices was to establish the key electrical parameters. This data was then used as the baseline to evaluate parameter drift in each of the device types after they had been subjected to all screening and stress tests.

Of the almost 4000 devices purchased for the Beam Lead Reliability portion of the study, 45 were selected for detailed electrical test: 5 of each type of the nine devices previously identified. The devices were selected randomly and screened to detect shorts, opens, or other gross mechanical defects. Only devices that were good were used to obtain electrical test data.

The purpose of the electrical test was threefold: (1) to check whether the manufacturer was meeting his published specifications, (2) to determine the "envelope" of the electrical characteristics, and (3) to make a baseline of data for later comparison, i.e., after the devices had been through all the screening and stress tests.

The purchased devices were first put on headers, categorized, and assigned a device code number for identification during the study. Because of the differences in configuration between manufacturers (and in some cases, between the same manufacturer's different production runs), the devices were characterized by pin configuration. This is shown in Table 4. All electrical tests were then conducted under conditions specified in each manufacturer's data sheet. The definition of symbols for the test parameters is listed opposite. The actual measured device parmaters, along with the specification limits for each parameter, are given for each of the nine devices in Tables 5 through 13. These initial device parameters are later compared with the parameters measured on the device survivors at the end of all the screen/stress tests.

DEFINITIONS OF SYMBOLS

A_{VOL}	Open Loop voltage gain
I_F	Input forward current
I_{IL}	Low level input current
I_{IH}	High level input current
I_{IO}	Input offset current
I_{PDH}	Power supply current drain with inputs in Logic "1" state
I_{PDL}	Power supply current drain with inputs in Logic "0" state
I_{R1}	Input reverse current with V_{IH} applied
I_{R2}	Input reverse current with V_{IHH} applied
I_{SC}	Logic "1" state source current with output shorted to ground
V_{IC}	Maximum negative voltage at input continuous or pulsed
V_{IH}	Logic "1" state input voltage
V_{IHH}	Input breakdown voltage
V_{IL}	Logic "0" state input voltage
V_{IO}	Input offset voltage
V_{OH}	Output voltage high
V_{OL}	Output voltage low
$V_{swing}(V_O)$	Output voltage swing

TABLE 4. TABLE OF DEVICE PIN CONFIGURATIONS

Beam Lead Pin Numbers*	SC148/Digital/5473	SC149/Digital/RF100	SC150/Digital/5400	SC151/Digital/5410	SC152/Linear/741	SC153/Linear/741	SC154/Linear/741	SC155/Linear/RM101	SC156/Linear/710
	W	X	W	Z	W	Y	Z	X	W
1	Clock A	K_A	Input 1B	Input 1A	NC	NC	Offset Null 2	Balance	GND
2	Reset B	J_A	Output 1	Output 1	NC	NC	NC	NC	+Input
3	K_A	Clock A	V_{CC}	V_{CC}	Offset-Null	NC	Output	Output	-Input
4	V_{CC}	V_{CC}	Output 2	Output 2	-Input	NC	Comp.	NC	NC
5	Clock B	Clock A	Input 2A	Input 2A	+Input	NC	NC	NC	V_{EE}
6	Reset B	J_B	Input 2B	Input 2B	V_{EE}	V_{CC}	$+V_{CC}$	V_{CC}	NC
7	J_B	K_B	Output 3	Input 2C	NC	NC	NC	NC	Output
8	---	Set B	Input 3A	Input 3A	NC	Output	NC	NC	NC
9	---	Q_B	Input 3B	Input 3B	NC	NC	Comp.	Comp.	V_{CC}
10	---	GND	GND	GND	NC	NC	NC	NC	NC
11	---	Q_B	Input 4A	Input 3C	Offset Null	NC	Offset Null 1	Comp. Bal	NC
12	---	Q_A	Input 4B	Output 3	Output	Offset Null	NC	NC	NC
13	Q_B	Q_A	Output 4	Input 1B	V_{CC}	$-V_{CC}$	-Input	-Input	---
14	Q_B	Set A	Input 1A	Input 1C	NC	NC	NC	NC	---
15	K_B	---	---	---	NC	NC	NC	NC	---
16	GND	---	---	---	NC	NC	+Input	+Input	---
17	Q_A	---	---	---	NC	+Input	NC	NC	---
18	Q_A	---	---	---	NC	+Input	NC	NC	---
19	J_A	---	---	---	---	-Input	$-V_{CC}$	$-V_{CC}$	---
20	NC	---	---	---	---	NC	NC	NC	---
21	NC	---	---	---	---	NC	---	---	---
22	NC	---	---	---	---	Offset Null	---	---	---
23	NC	---	---	---	---	---	---	---	---
24	NC	---	---	---	---	---	---	---	---

*Beam Lead Pin numbers are labeled counterclockwise from Pin 1 except for SC149 which is labeled clockwise from Pin 1. All chips are mounted face down.

+Input non-inverting Input
-Input Inverting Input

NC: no connection to pin

TABLE 5. ELECTRICAL CHARACTERIZATION OF THE SC148 DUAL J-K FLIP FLOP (5473) FROM VENDOR W

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\bar{X}$)	Standard Deviation
1	V_{OH}	>2.4V	18	3.030	0.017
2			18	3.032	0.017
3			17	3.069	0.014
4			13	3.360	1.302
5			14	2.881	0.747
6	V_{OH}	>2.4V	13	3.361	1.302
7	V_{OL}	<0.4V	17	0.251	0.025
8			17	0.256	0.013
9			18	0.286	0.019
10			14	0.255	0.013
11			13	0.345	0.282
12	V_{OL}	<0.4V	14	0.256	0.012
13	I_{RI}	<80μA	1	-0.210μA	0.074
14		<40μA	19	0.002	0.000
15		<40μA	3	0.008	0.022
16		<80μA	5	-0.220	0.052
17		<40μA	7	0.013	0.030
18	I_{RI}	<40μA	15	0.003	0.001
19	I_F	<-3.2mA	1	-0.872	0.038
20		-1.6mA	19	-1.001	0.237
21		<-1.6mA	3	-1.318	0.314
22		<-3.2mA	5	-1.125	0.267
23		<-1.6mA	7	-1.162	0.467
24	I_F	<-1.6mA	15	-1.244	0.429
25	I_{RI}	<80μA	2	0.012	0.003
26	I_F	<-3.2mA	2	-1.381	0.034
27	I_{CC}	40mA	4	28.939	2.330
28	I_{RI}	<80μA	6	0.006	0.022
29	I_F	<-3.2mA	6	-1.378	0.079

TABLE 6. ELECTRICAL CHARACTERIZATION OF THE SC149 DUAL J-K FLIP FLOP (RF 100) FROM VENDOR X

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\bar{X}$)	Standard Deviation
1	I_{IL}	<-1.33mA	3	-0.969	0.022
2	I_{IH}	<0.14	3	0.010	0.004
3	V_{OH}	>3.0V	13	3.430	0.023
4	I_{IL}	<-1.33mA	5	-0.984	0.031
5	I_{IH}	<0.14	5	0.010	0.005
6	V_{OH}	>3.0V	9	3.433	0.025
7	I_{IL}	<-2.4mA	14	-1.501	0.048
8	I_{IH}	<0.07mA	14	0.000	0.000
9	V_{OH}	>3.0V	13	3.365	0.013
10	I_{IL}	<-2.4mA	8	-1.371	0.472
11	I_{IH}	<0.07	8	0.000	0.000
12	V_{OH}	>3.0V	9	3.376	0.011
13	I_{IL}	<-1.33mA	6	-0.843	0.061
14	I_{IH}	<0.07	6	0.005	0.002
15	V_{OH}	>3.0V	11	3.340	0.022
16	I_{IL}	<-1.33mA	2	-0.859	0.059
17	I_{IH}	<0.07	2	0.005	0.002
18	V_{OH}	>3.0V	12	3.336	0.016
19	I_{IL}	<-1.33mA	1	-1.092	0.025
20	I_{IH}	<0.07	1	0.005	0.003
21	I_{CC}	<28	4	21.044	0.925
22	I_{IL}	<-1.33mA	7	-1.112	0.031
23	I_{IH}	<0.07mA	7	0.004	0.002
24	I_{CC}	<28mA	4	21.225	0.933
25	V_{OL}	<0.4V	13	0.159	0.020
26		↓	12	0.138	0.016
27			12	0.145	0.017
28			9	0.133	0.017
29			11	0.135	0.017
30			11	0.141	0.017

TABLE 7. ELECTRICAL CHARACTERISTICS OF THE SC150 QUAD 2 INPUT NAND GATE (5400) FROM VENDOR W

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\overline{X}$)	Standard Deviation
1	V_{OH}	>2.4V	2	2.824	0.014
2			2	2.737	0.014
3			4	2.734	0.013
4			4	2.734	0.013
5			7	2.744	0.022
6			7	2.745	0.022
7			13	2.738	0.015
8	V_{OH}	>2.4V	13	2.738	0.014
9	V_{OL}	<0.4V	2	0.308	0.411
10			4	0.214	0.011
11			7	0.212	0.012
12	V_{OL}	<0.4V	13	0.221	0.013
13	I_{RI}	<40μA	14	0.003	0.001
14			1	0.004	0.004
15			5	0.004	0.001
16			6	0.004	0.001
17			8	0.003	0.001
18			9	0.004	0.002
19			11	0.003	0.001
20	I_{RI}	<40μA	12	0.003	0.001
21	I_{R2}	<1.0mA	14	0.005	0.002
22			1	0.010	0.022
23			5	0.005	0.002
24			6	0.005	0.002
25			8	0.005	0.002
26			9	0.005	0.002
27			11	0.005	0.002
28	I_{R2}	<1.0mA	12	0.005	0.001
29	I_F	<-1.6mA	14	-1.221	0.069
30			1	-1.221	0.069
31			5	-1.238	0.067
32			6	-1.237	0.067
33			8	-1.223	0.066
34			9	-1.223	0.066
35			11	-1.226	0.068
36	I_F	<-1.6mA	12	-1.226	0.068

TABLE 7. ELECTRICAL CHARACTERISTICS OF THE SC150 QUAD 2 INPUT NAND GATE (5400) FROM VENDOR W (Continued)

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\bar{X}$)	Standard Deviation
37	V_{IC}	<-1.5V	14	-0.984	0.015
38			1	-1.000	0.016
39			5	-0.996	0.016
40			6	-0.983	0.015
41			8	-0.987	0.016
92			9	-0.950	0.013
43			11	-0.989	0.017
44	V_{IC}	<-1.5V	12	-0.949	0.013
45	I_{SC}	>-20mA	2	-42.114	1.177
46		<-55mA	4	-41.772	1.039
47			7	-41.865	1.166
48			13	-42.164	1.116
49			2	-42.060	1.169
50			4	-41.735	1.033
51			7	-41.832	1.159
52	I_{SC}	<-55mA	13	-42.138	1.113
53	I_{PPL}	<8.0mA	3	5.386	0.284
54	I_{PPH}	<22 mA	3	19.856	0.719

TABLE 8. ELECTRICAL CHARACTERIZATION OF THE SC151 TRIPLE 3 INPUT NAND GATE (5410) FROM VENDOR Z

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\bar{X}$)	Standard Deviation
1	V_{OL}	<0.4V	2	0.265	0.012
2			4	0.262	0.013
3	V_{OL}	<0.4V	12	0.263	0.012
4	V_{OH}	>2.4V	2	2.751	0.019
5			2	2.729	0.020
6			4	2.720	0.024
7			4	2.745	0.020
8			4	2.720	0.023
9			12	2.738	0.031
10			12	2.760	0.031
11			12	2.742	0.034
12	V_{OH}	>2.4V	2	2.727	0.020
13	I_{IL}	<-1.6mA	14	-1.268	0.032
14			1	-1.268	0.034
15			5	-1.275	0.023
16			6	-1.275	0.021
17			7	-1.275	0.022
18			8	-1.332	0.037
19			9	-1.333	0.036
20			11	-1.334	0.039
21	I_{IL}	<-1.6mA	13	-1.267	0.034
22	I_{IH}	<40μA	14	0.013	0.004
23			1	0.007	0.002
24			5	0.006	0.003
25			6	0.012	0.004
26			7	0.007	0.003
27			8	0.009	0.003
28			9	0.013	0.005
29			11	0.007	0.003
30	I_{IH}	<40μA	13	0.008	0.002
31	I_I	<1.0mA	14	0.019	0.007
32			1	0.010	0.004
33			5	0.010	0.006
34			6	0.018	0.008
35			7	0.011	0.006
36			8	0.013	0.005
37			9	0.021	0.009
38			11	0.011	0.005
39	I_I	<1.0mA	13	0.012	0.005

TABLE 8. ELECTRICAL CHARACTERIZATION OF THE SC151 TRIPLE 3 INPUT NAND GATE (5410) FROM VENDOR Z (Continued)

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\bar{X}$)	Standard Deviation
40	I_{OS}		2	-31.024	0.939
41	|	-18mA to	4	-30.966	0.836
42	|	-55mA	12	-30.331	0.801
43	|	|	2	-31.012	0.932
44	|	-18 mA to	4	-30.971	0.832
45	I_{OS}	-55 mA	12	-30.333	0.798
46	I_{CCL} Total	<16.5mA	3	11.789	0.187
47	I_{CCH} Total	<6mA	3	4.024	0.063

TABLE 9. ELECTRICAL CHARACTERISTICS OF THE SC152 OPERATIONAL AMPLIFIER (741) FROM VENDOR W

	Specifications			Measured Value	
Test Number	Test Parameter	Spec. Value	Pin Under Test	Mean ($\overline{X}$)	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤5 mv	4, 5	-1.708	1.568
2	$\lvert I_{IO} \rvert$	≤200 nA	4, 5	-0.871	34.122
3	A_{VOL}	≥50 K	12	110,478	17,693
4	V_{swing}	≥±12 V	12	13.503	0.300
5				-12.743	0.092

TABLE 10. ELECTRICAL CHARACTERISTICS OF THE SC153 OPERATIONAL AMPLIFIER (741) FROM VENDOR Y

	Specifications			Measured Value	
Test Number	Test Parameter	Spec. Value	Pin Under Test	Mean ($\overline{X}$)	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤5 mv	18, 19	0.805	2.131
2	$\lvert I_{IO} \rvert$	≤200 nA	18, 19	-0.270	7.068
3	A_{VOL}	≥50,000	8	122,068	7,303
4	V_{swing}	≥±12 V	8	13.488	0.047
5			5	-12.687	0.063

TABLE 11. ELECTRICAL CHARACTERISTICS OF THE SC154 OPERATIONAL AMPLIFIER (741) FROM VENDOR Z

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\overline{X}$)	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤5 mv	13, 16	1.711	3.239
2	$\lvert I_{IO} \rvert$	≤200 nA	13, 16	0.065	11.661
3	A_{VOL}	≥50,000	3	127,022	8,973
4	V_{swing}	≥±12 V	3	13.283	1.370
5	V_{swing}	≥±12 V	3	-12.200	3.754

TABLE 12. ELECTRICAL CHARACTERISTICS OF THE SC155 OPERATIONAL AMPLIFIER FROM VENDOR X

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\overline{X}$)	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤5 mv	13, 16	-2.055	16.126
2	$\lvert I_{IO} \rvert$	≤200 nA	13, 16	29.981	67.258
3	A_{VOL}	≥50,000	3	124,311	9,852
4	V_{swing}	≥±12 V	3	12.751	3.789
5	V_{swing}	≥±12 V	3	-13.527	3.891

TABLE 13. ELECTRICAL CHARACTERISTICS OF THE SC156 VOLTAGE COMPARATOR (710) FROM VENDOR W

Test Number	Specifications		Pin Under Test	Measured Value	
	Test Parameter	Spec. Value		Mean ($\overline{X}$)	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤2 mv	2, 3	0.445	0.928
2	$\lvert I_{IO} \rvert$	≤5 μA	2, 3	-0.277	0.902
3	A_{VOL}	>1250	7	72,845	70,398
4	V_{OH}	2.5 - 4.0 V	7	2.880	0.146
5	V_{OL}	-1.0 to 0.0 V	7	-0.191	0.240

3. CHARACTERIZING THE DEVICES ACCORDING TO PHYSICAL PARAMETERS

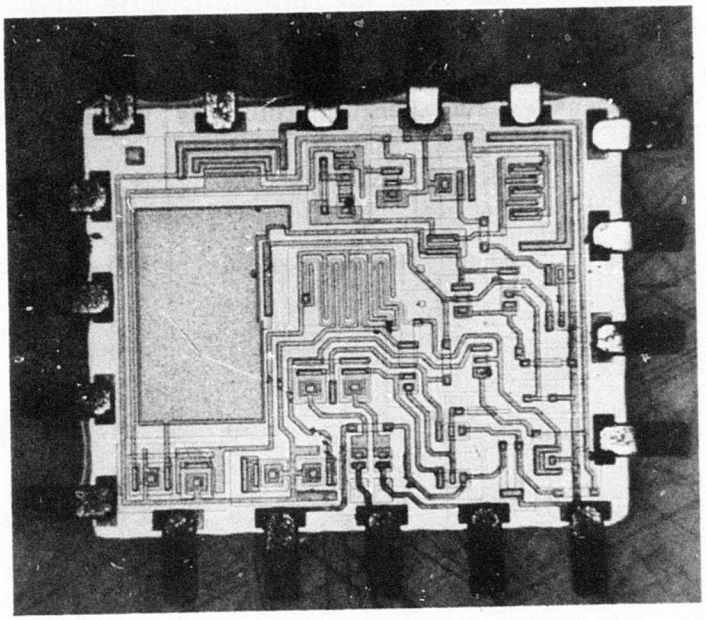
Physical inspection, including both precise dimensioning and visual examination of both geometry and topology, was undertaken in order to compare manufacturing differences and to relate any specific physical characteristic with subsequent failure data.

In parallel with the electrical test described in the previous topic, a sample of 90 devices (10 per vendor, per device type) was measured per MIL-STD-883, Method 2008A. Table 14 details the external physical device characteristics. The dimensions cited in the table are the average (mean) for each type. Note the lack of standardization among vendors; within even such a widely used device as the uA 741 operational amplifier, the number of pins vary from 10 to 20, and the beam width from 0.003 to 0.004 inch.

Photographs were made of the top of each different device type to detail the differences in metal interconnection schemes from vendor to vendor. These are shown in Figures 1 through 9 on the pages following.

TABLE 14. DEVICE PHYSICAL DIMENSIONS (IN THOUSANDTH OF INCH)

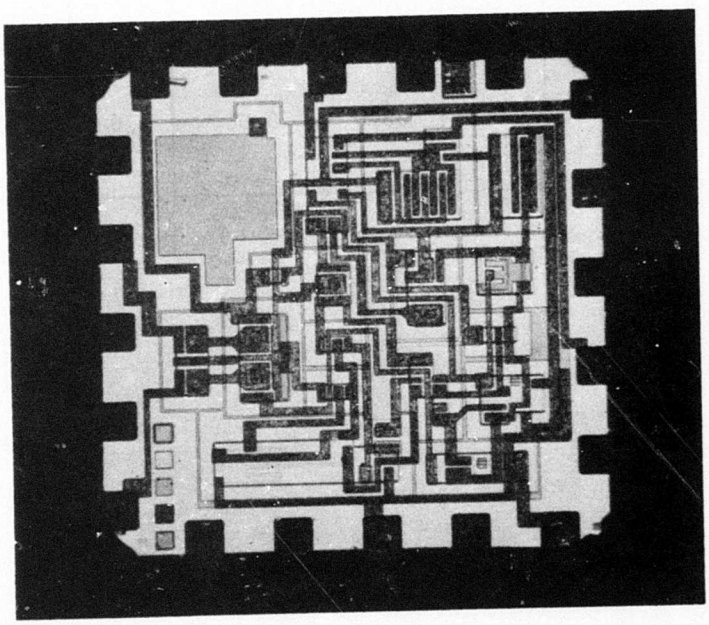
Device Code/ Group/Type	Vendor Code	Dice Thickness	Dice Width	Dice Length	Beam Thickness	Beam Width	Number of Beam
SC148/Digital/ 5473	W	2.4	64.0	64.7	0.66	3.0	24
SC149/Digital/ RF100	X	5.3	53.0	63.0	0.60	3.0	16
SC150/Digital/ 5400	W	2.1	34.0	44.0	0.71	4.0	14
SC151/Digital/ 5410	Z	2.4	32.4	42.2	0.49	3.0	14
SC152/Linear/ 741	W	2.3	42.7	52.9	0.33	3.0	18
SC153/Linear/ 741	Y	2.5	52.8	62.7	0.51	3.2	10
SC154/Linear/ 741	Z	2.3	53.4	53.5	0.47	3.0	20
SC155/Linear/ RM101	X	4.7	55.0	57.0	0.50	4.0	20
SC156/Linear/ 710	W	3.0	33.0	33.0	0.63	3.0	12



49174-36

GROUP — LINEAR
VENDOR — W
TYPE — 741
COMPLEXITY FACTOR — SIMPLE
NOMINAL SIZE — .043" X .053"

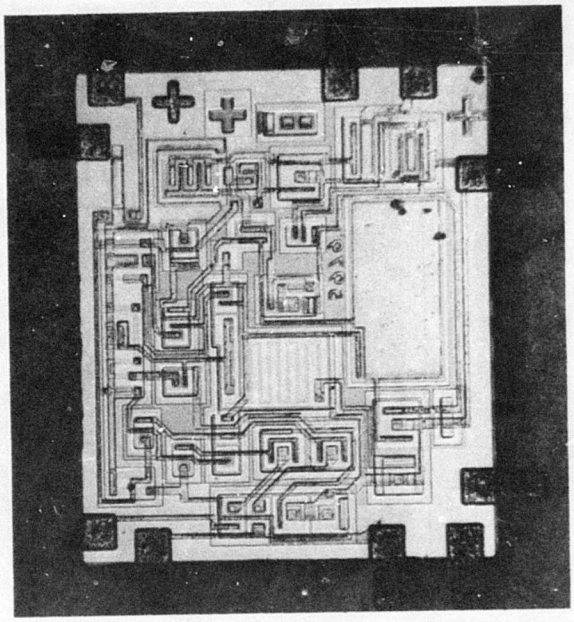
Figure 1. Operational Amplifier: Code – SC152



49174-33

GROUP — LINEAR
VENDOR — X
TYPE — RM101
COMPLEXITY FACTOR — SIMPLE
NOMINAL SIZE — .055" X .057"

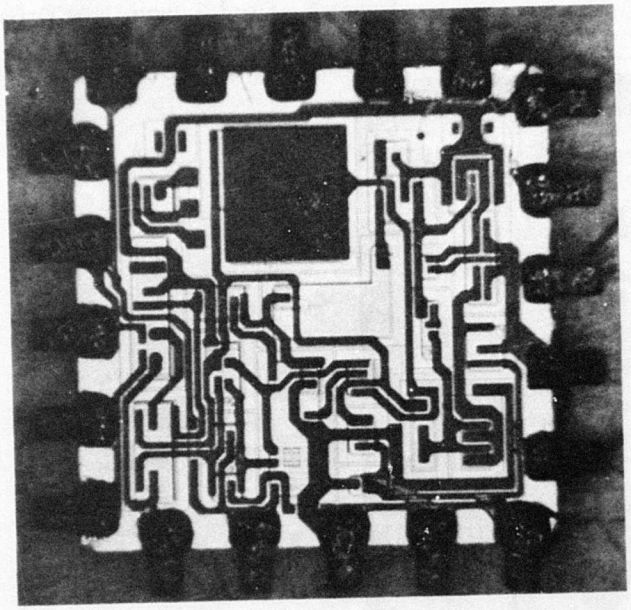
Figure 2. Operational Amplifier: Code – SC155



49174-35

GROUP — LINEAR
VENDOR — Y
TYPE — 741
COMPLEXITY FACTOR — SIMPLE
NOMINAL SIZE — .053" X .063"

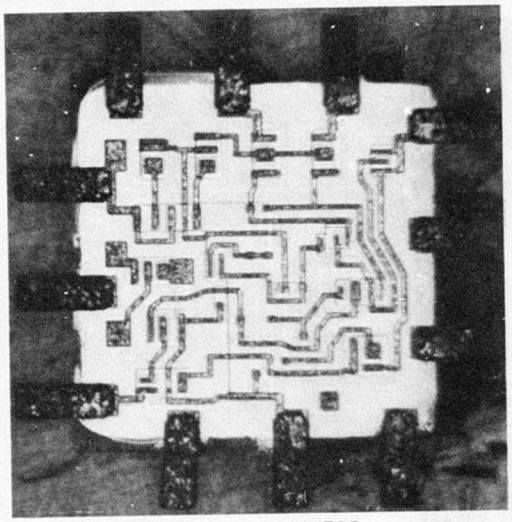
Figure 3. Operational Amplifier: Code – SC153



49174-34

GROUP — LINEAR
VENDOR — Z
TYPE — 741
COMPLEXITY FACTOR — SIMPLE
NOMINAL SIZE — .053" X .053"

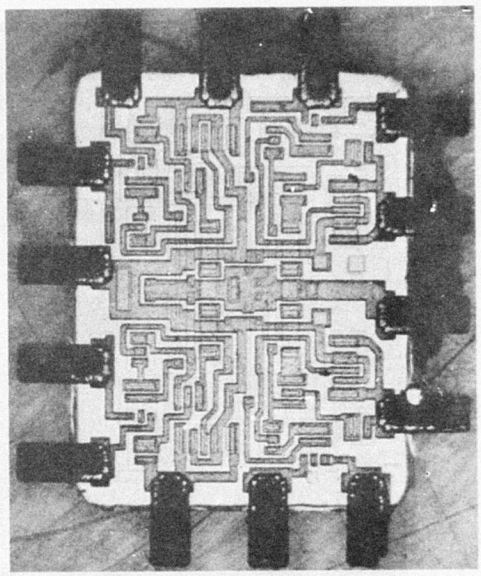
Figure 4. Operational Amplifier: Code – SC154



49174-32

GROUP	— LINEAR
VENDOR	— W
TYPE	— 710
COMPLEXITY FACTOR	— COMPLEX
NOMINAL SIZE	— .033" X .033"

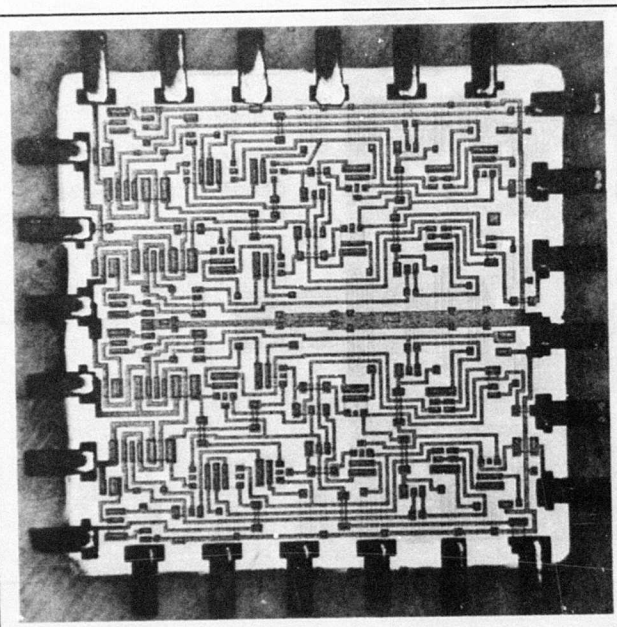
Figure 5. Voltage Comparator: Code – SC156



49174-38

GROUP	— DIGITAL
VENDOR	— W
TYPE	— 5400
COMPLEXITY FACTOR	— SIMPLE
NOMINAL SIZE	— .034 INCHES X .044 INCHES

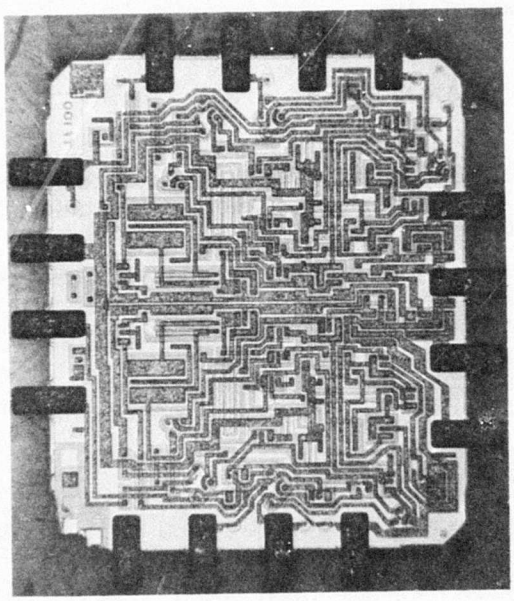
Figure 6. Quad 2 Input NAND Gate: Code – SC150



49174-31

GROUP	— DIGITAL
VENDOR	— W
TYPE	— 5473
COMPLEXITY FACTOR	— COMPLEX
NOMINAL SIZE	— .064 INCHES X .064 INCHES

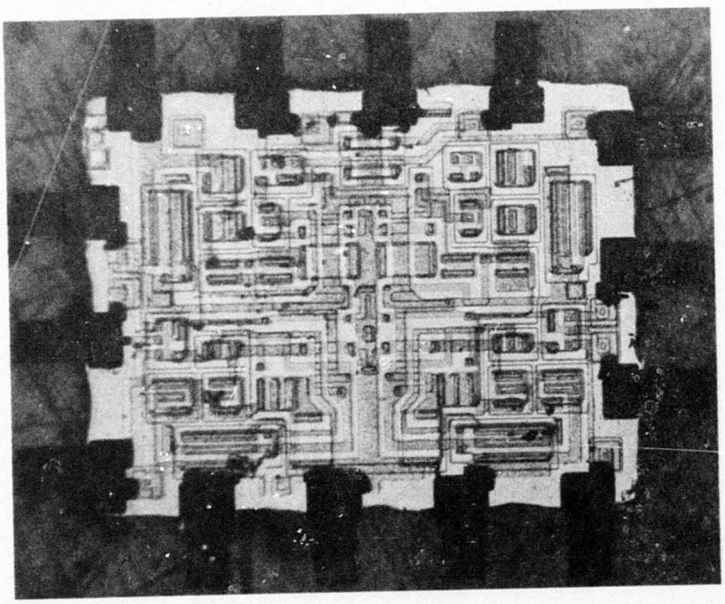
Figure 7. Dual J-K Flip-Flop: Code SC148



49174-39

GROUP — DIGITAL
VENDOR — X
TYPE — RF 100
COMPLEXITY FACTOR — COMPLEX
NOMINAL SIZE — .053 INCHES X .063 INCHES

Figure 8. Dual J-K Flip-Flop: Code – SC149



49174-37

GROUP — DIGITAL
VENDOR — Z
TYPE — 5410
COMPLEXITY FACTOR — SIMPLE
NOMINAL SIZE — .032 INCHES x .042 INCHES

Figure 9. Triple 3 Input NAND Gate: Code – SC151

4. VISUALLY DETERMINED DEFECTS AND ANOMALIES

A random sampling of each device type was selected and visually inspected to determine the extent and nature of commonly occurring fabrication defects. The defects and anomalies discovered are listed and illustrated below.

Another sample of 90 devices (10 per vendor/type) were visually inspected at 100X magnification. The visual defects or anomalies for each device type are shown in Table 15 below. Photographs were made of several types of defects and are shown in Figures 10 through 20 on the following pages.

The number entry in the table indicates the defect frequency within each sample. Note that the most common defect was broken nitride over the beam.

TABLE 15. VISUAL DEFECTS OR ANOMALIES

	SC148	SC149	SC150	SC151	SC152	SC153	SC154	SC155	SC156
	Digital				Linear				
	5473 W	RF100 X	5400 W	5410 Z	741 W	741 Y	741 Z	RM101 X	741 W
Defects Inspected For	Defects Found								
Nitride Broken Over Beam	5	10	10	1	10	2	5	1	3
Crack in Nitride (>0.001 inches pointing to or in active area of device)	8								1
Holes in Nitride	2	3						1	1
Bent Beams (1/4 Beam Width; 30° vertical) Broken Beams							1		
Voids in Conductors	2								
Spalling Gold	5				1				
Shorts Between Adjacent Conductors	9			10					1
Discolored Gold			1		1			5	
Lifted or Separated Metal									
Gold Plating Anomalies									
Metal <75% of Design Width		1		1					
Deep Scratches				1					
Exposed Junctions									
Misaligned Patterns									

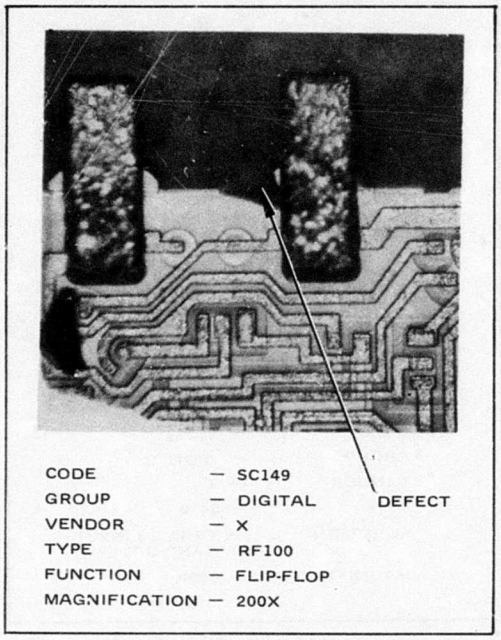


Figure 10. Nitride Broken Under Beam

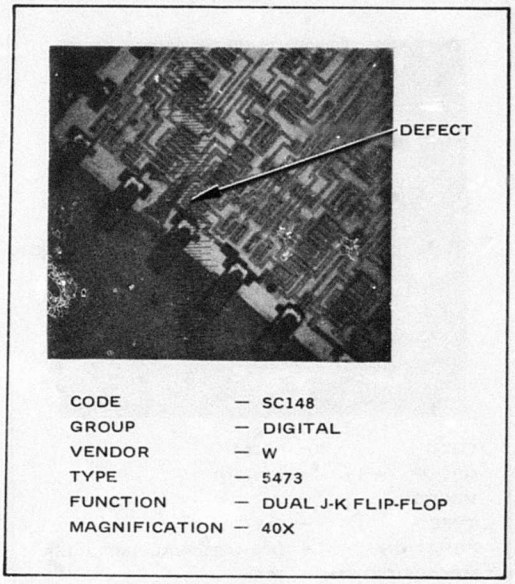


Figure 11. Broken Nitride

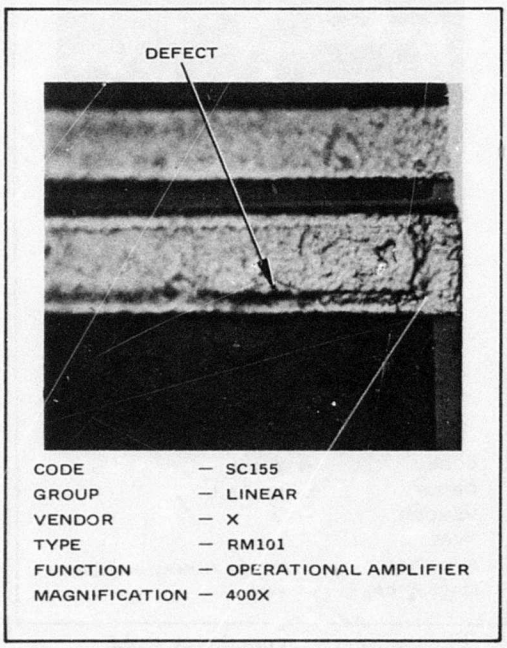


Figure 12. Hole in Nitride

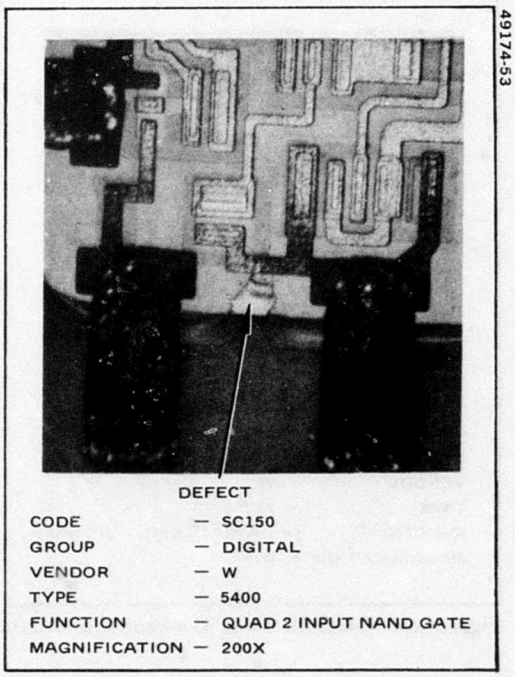
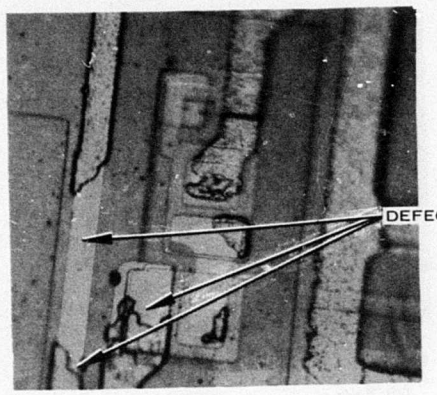


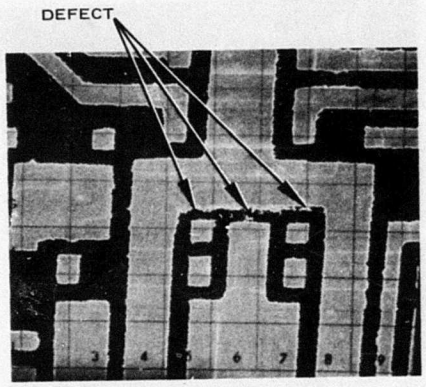
Figure 13. Crack in Nitride



49174-55

CODE — SC154
GROUP — LINEAR
VENDOR — Z
TYPE — 741
FUNCTION — OPERATIONAL AMPLIFIER
MAGNIFICATION — 200X

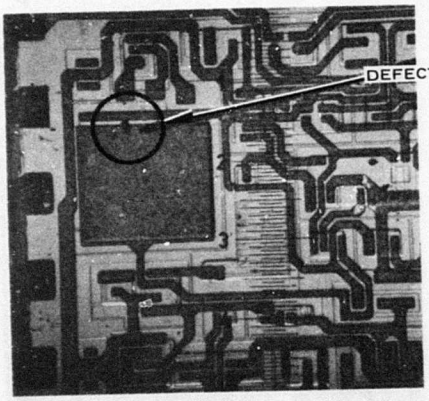
Figure 14. Voids in Conductor



49174-56

CODE — SC151
GROUP — DIGITAL
VENDOR — Z
TYPE — 5410
FUNCTION — TRIPLE 3 INPUT NANO GATE
MAGNIFICATION — 300X

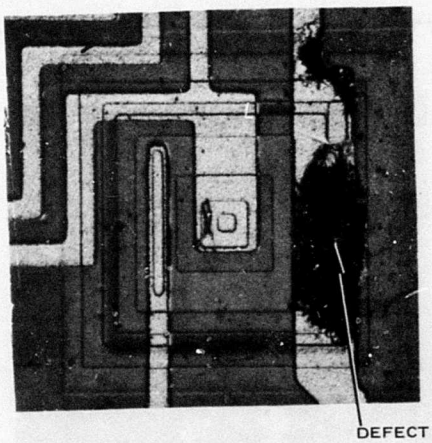
Figure 15. Spalling Gold



49174-57

CODE — SC152
GROUP — LINEAR
VENDOR — W
TYPE — 741
FUNCTION — OPERATIONAL AMPLIFIER
MAGNIFICATION — 40X

Figure 16. Gold Shorting Between Conductor



49174-58

CODE — SC153
GROUP — DIGITAL
VENDOR — Y
TYPE — 741
FUNCTION — OPERATIONAL AMPLIFIER
MAGNIFICATION — 200X

Figure 17. Discolored Gold

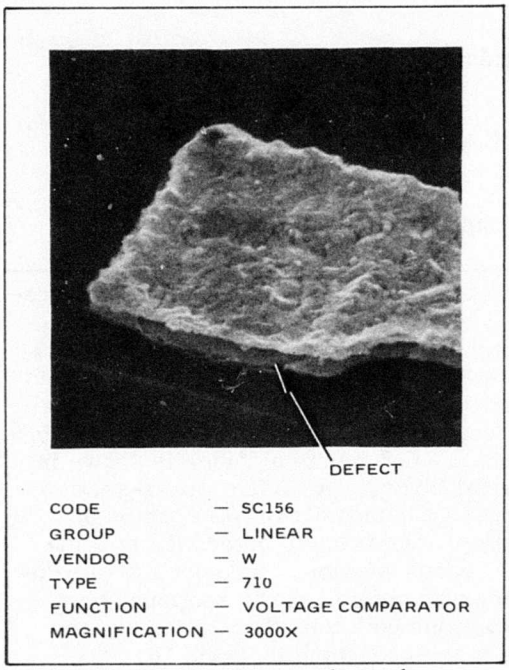


Figure 18. Separated Metal

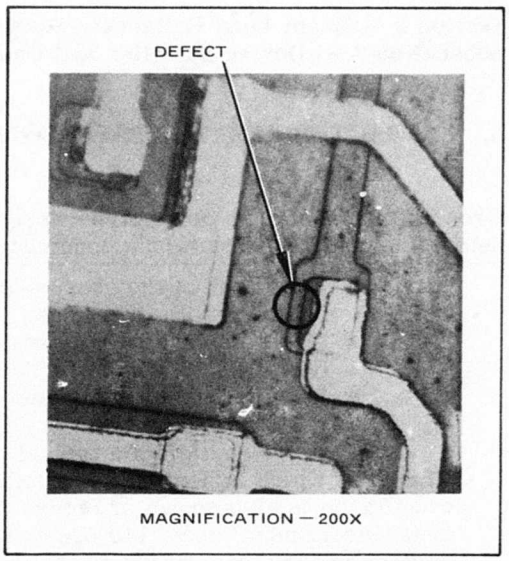


Figure 19. Exposed Junctions

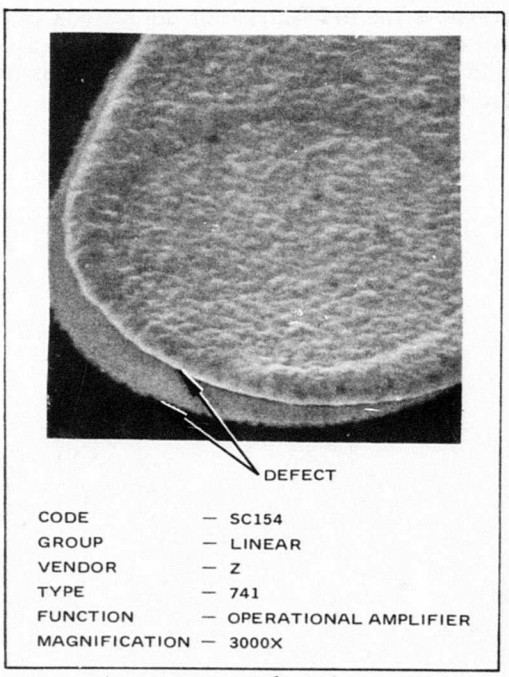


Figure 20. Misaligned Pattern

5. CHARACTERIZING THE BASELINE DEVICE MATERIAL

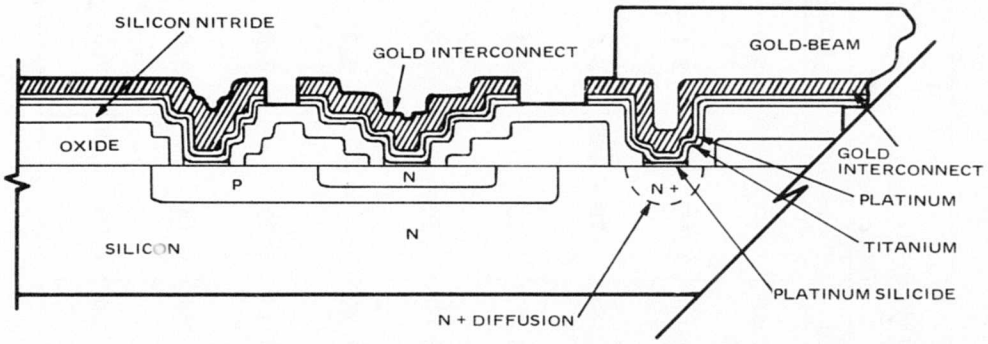
Cross sections of each device type were photographed and measured on the SEM to determine details of beam lead construction.

Examination of the cross section of each device type was undertaken to resolve the following four questions:

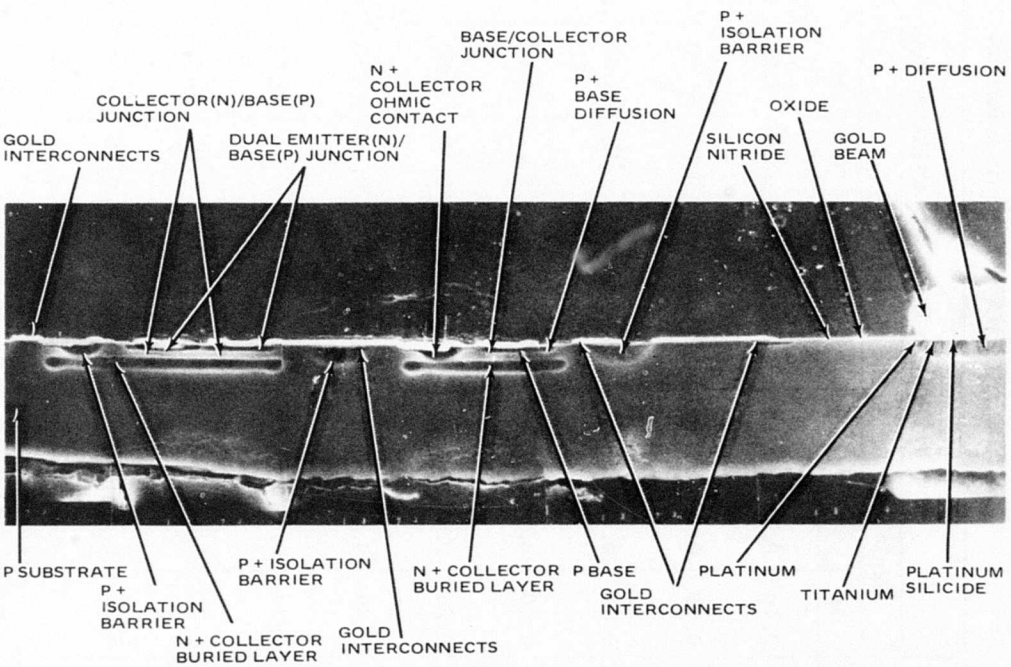
- Were the vendors following the Bell Labs metallurgy system?
- How did the beam lead structure vary from one manufacturer to another?
- How did each vendor meet his own requirements?
- What were the variations in device construction that affected reliability?

A cross-section of a typical beam lead sealed junction device is shown in Figure 21 which indicates the critical material layers. An actual cross-section of a device is also shown in Figure 21. This is a composite of SEM photos of cross-sections of an SC 149 (Dual J-K flip flop). In order to determine how the devices under study conformed to the typical cross-section, 18 devices (2 per device type) were analyzed. Here, each device was potted, cross-sectioned photographed and microprobed on the SEM to determine both the composition and the thickness of the material layers. These data are presented in Table 16. The measured material thickness values can be compared to the vendor target values shown in Table 16. Target values were obtained by verbal communication with each beam lead device supplier.

Table 17 indicates the orientation of the silicon in the 9 devices. A possible correlation between channeling failures and crystal orientation was under scrutiny because this type of failure is reported to be prevalent in devices made from <100> oriented silicon.



(a) Desired Cross-Section Fabricated According to Bell Labs Metallurgical Requirements (Thickness Exaggerated for Clarity)



(b) SEM Photograph of Beam Lead Device Cross-Section (Dual J-K Flip-Flop) Showing Interconnect Metallurgy and Device Junctions

Figure 21. Cross-Section of a Typical Beam Lead Device

TABLE 16. COMPARISON OF MEASURED VS "TARGET" THICKNESS OF BEAM LEAD DEVICE MATERIAL (in microns)

Device Code/ Group/Type	Mfr	Material Thickness (Measured, M, and Target, T)										
		Oxide		Si_3N_4		Pt		Ti		Interconnect Gold		
		M	T	M	T	M	T	M	T	M	T(vacuum)	T(plated)
SC148/Digital/ 5473	W	0.70	0.50	0.10	0.20	0.10	0.15	0.30	0.11	2.30	0.70 - 1.00	3.0
SC149/Digital/ RF100	X	0.40	0.10	0.10	0.12 -0.18	0.10	0.35	0.30	0.11	0.20	0.15	2.0 - 4.0
SC150/Digital/ 5400	W	0.50	0.50	0.20	0.20	0.20	0.15	0.60	0.11	1.35	0.70 - 1.00	3.0
SC151/Digital/ 5410	Z	0.40	0.50	0.20	0.20	0.10	*	0.70	*	0.35	0.25	2.5
SC152/Linear/ 741	W	0.90	0.50	0.15	0.20	0.05	0.15	0.20	0.11	2.00	0.70 - 1.00	3.0
SC153/Linear/ 741	Y	0.60	0.60	0.18	0.18	0.05	0.12	0.15	0.12	2.20	---	2.0
SC154/Linear/ 741	Z	0.30	0.50	0.20	0.20	0.15	*	0.60	*	2.70	0.25	2.5
SC155/Linear/ RM101	X	0.50	0.10	0.20	0.12 -0.18	0.10	0.35	0.40	0.15	1.65	0.15	2.0 - 4.0
SC156/Linear/ 710	W	0.50	0.50	0.18	0.20	0.10	0.15	0.90	0.11	1.10	0.70 - 1.00	3.0

*0.3 total for both Pt and Ti target.
Note: Accuracy at measured thickness is ± 0.025 microns

TABLE 17. SILICON ORIENTATION OF MATERIAL

Device Code	Device Group	Device Type	Vendor	Si Orientation
SC148	Digital	5473	W	< 111 >
SC149	Digital	RF100	X	< 100 >
SC150	Digital	5400	W	< 111 >
SC151	Digital	5410	Z	< 111 >
SC152	Linear	741	W	< 111 >
SC153	Linear	741	Y	< 100 >
SC154	Linear	741	Z	< 111 >
SC155	Linear	RM101	X	< 100 >
SC156	Linear	710	W	< 111 >

6. MEASURING THE BEAM'S PHYSICAL CHARACTERISTICS

A sample of 90 devices (2 per vendor, per type, per test) was measured for the following physical characteristics: beam hardness, beam peel strength, beam shear strength, lead bend, and lead fatigue. Comparison of the data obtained indicates some wide variations in the mean values in devices, even from the same vendor.

Of the five tests conducted on the 90 device, beam hardness has a direct relationship to the bonding of beam leads to the substrate. (The other four tests were standard hybrid package qualification tests.) All devices were tested to destruction.

Beam Hardness — The beam hardness of each device type was measured using a knoop hardness test with a 5-gram load. The knoop hardness number for each device type is shown in Table 18. Note the range of mean hardness varies from a low of 38.7 (vendor X) to a high of 63.4 (vendor Z).

Beam Peel Strength — The beam peel strength test was done by modifying an Engineering Associates Wire Bond Tester so that the shear gage could be clamped directly to a given beam of the device. The beam peel angle was 90 degrees with relation to the top of the device. Values for each device type are given in Table 19. Note that vendor W shows a variation in mean from 6.1 (linear device) to 8.3 (digital device), which means a probable variation between device processing lines.

Beam Shear Strength — The beam shear strength tests were done on the same test set up and proccdure as the beam peel tests. Note (from Table 19) that the mean force ranges from a low of 15.3 to a high of almost 24.

Lead Bend and Lead Fatigue — The lead bend test was performed per MIL-STD-883, Method 2004, Condition B1. The combined weight of the clamp and the affixed weight was two grams and the lead was bent through one cycle. The lead fatigue test testing, (Method 2004, Condition B2), was performed in a similar manner except that the lead was bent through 3 cycles.

The results of visual examination of the devices after the lead bend and lead fatigue tests are given in Table 20. Note that for Vendor Z, no damage was observed for the lead fatigue tests. This correlates with the high shear strength data shown in Table 19 for this vendor.

TABLE 18. RESULTS OF BEAM HARDNESS TEST

Device Code	Device Group	Device Type	Vendor	Knoop Hardness Number		
				High	Low	Mean
SC148	Digital	5473	W	50.6	37.6	42.0
SC149	Digital	RF100	X	61.5	45.6	52.6
SC150	Digital	5400	W	74.1	49.3	59.9
SC151	Digital	5410	Z	72.3	54.1	62.6
SC152	Linear	741	W	46.8	33.6	38.8
SC153	Linear	741	Y	69.5	37.5	53.9
SC154	Linear	741	Z	71.7	53.4	63.4
SC155	Linear	RM101	X	39.5	37.6	38.7
SC156	Linear	710	W	46.8	40.3	46.1

TABLE 19. RESULTS OF BEAM STRENGTH TESTS

Device Code	Device Group	Device Type	Vendor	Peel Strength (grams)			Beam Shear Strength (grams)		
				High	Low	Mean	High	Low	Mean
SC148	Digital	5473	W	10.0	5.0	7.3	18.0	13.0	15.3
SC149	Digital	RF100	X	8.0	6.0	7.0	20.0	16.0	18.0
SC150	Digital	5400	W	9.5	7.0	8.3	19.0	11.0	16.1
SC151	Digital	5410	Z	8.0	4.0	6.6	18.5	16.0	17.1
SC152	Linear	741	W	8.0	7.0	7.6	25.0	11.0	17.0
SC153	Linear	741	Y	8.0	6.0	6.8	21.5	10.0	17.7
SC154	Linear	741	Z	8.0	6.5	6.5	26.0	21.0	23.8
SC155	Linear	RM101	X	8.5	6.0	6.9	18.0	15.0	17.0
SC156	Linear	710	W	6.5	4.5	6.1	22.5	16.0	18.3

TABLE 20. RESULTS OF VISUAL EXAMINATION AFTER LEAD BEND AND LEAD FATIGUE

Device Code	Device Group	Device Type	Vendor	Lead Bend Visual @ 40X	Lead Fatigue Visual @ 40X Beam Width Broken
SC148	Digital	5473	W	No damage observed	10%
SC149	Digital	RF100	X	No damage observed	10%
SC150	Digital	5400	W	No damage observed	10%
SC151	Digital	5400	Z	No damage observed	No damage observed
SC152	Linear	741	W	No damage observed	10%
SC153	Linear	741	Z	No damage observed	15%
SC154	Linear	741	Z	No damage observed	No damage observed
SC155	Linear	RM101	X	No damage observed	10%
SC156	Linear	710	W	No damage observed	15%

7. RESULTS OF THE THERMAL MAPPING ANALYSIS

To pinpoint the nature of heat-related failures of IC devices, a detailed thermal analysis of the purchased beam lead devices was undertaken. Temperature gradient plots were constructed for the various devices to determine the high-temperature locations for subsequent comparison with observed failures.

Ideally the layout of an IC should be such that the temperature gradients across it are uniform, with no "hot spots" occurring. Further, it has been established that when high localized temperatures occur on an IC, those areas are more prone to fail than cooler areas. In the case of beam lead devices, thermal dissipation has long been recognized as one of the limiting factors in their use. It is common practice for hybrid manufacturers to inject a thermally conductive polymer into the air gap between device and substrate (bug-up region) to enhance thermal transfer. At least one manufacturer visited during the course of the study, in order to get acceptable hybrid operation, had to resort to direct mounting of a hot running beam lead device (metallization-up) to the substrate and subsequently thermocompression bonded fron beam to substrate to make electrical connection pin-to-pin.

Thus recognizing these inherent thermal problems with beam lead devices, thermal maps were made of each device type obtained from each manufacturer. Here the purpose of collecting infrared thermal data was to detect hot spots on the surface of the dice and then to correlate these hot spots with failures from the screen/stress tests. During thermal mapping the Θ_{js} junction-to-substrate thermal resistance measurements were made on each device type for two orientattions, as shown in Figure 22. Figure 22a shows the face-down (metallization down) orientation. This is the normal beam lead device-to-substrate mounting configuration. However, in this configuration, the active surface cannot be seen by the IR microscope. Figure 22b shows the face-up (metallization-up) orientation. Here the back of the dice is mounted to the substrate with a thermally conductive adhesive. Electrical contact is made to the device by thermocompression gold ball bonds between each beam on the device and the appropriate substrate conductive pad.

Figures 23 through 44 illustrate the results of the thermal mapping. As previously stated, in the normal beam lead mounting configuration (Figure 22a), junction temperatures cannot be made using an IR microscope since the active metallized surface is hidden from view. Therefore, the temperature of the hottest spot on the back side of the device was used to calculate Θ_{js}. It is apparent from the uniform temperature profiles that the heat dissipated on the hidden metallized surface is spread significantly by the chip material. In the normal beam lead mounting mode, most of the heat is transferred through the beams to the substrate, hence very little heat is transferred from the active surface to the back surface. This is due to the thermal resistance of the chip which is a function of its thickness, thermal conductivity and size. Since junctions and other hot

spots cannot be seen from the back side, the device was bonded upside down (as in Figure 22b) in order that hot spots on the surface of the device could be viewed. In this orientation, the primary route for heat dissipation from the device will be from the device body, through the adhesive, into the substrate, while the secondary route of heat transfer is through the beams.

Nine types of beam lead devices, both analog (linear) and digital, were tested. Temperatures were measured on each device by scanning the surface with an infrared microscope, Sierra Electronics Division of Philco-Ford Model 700A. The infrared microscope measures radiant energy from a 1.3-mil diameter spot. The surface to be analyzed was first coated with a paint having a high termal emissivity. The paint used was a water-base black liquid-crystal undercoat VL-407-K, manufactured by the Vari-light Corporation, Cincinnati, Ohio. The temperatures recorded have a $\pm 0.5^{o}C$ tolerance.

Test circuit cards were constructed permitting the power to be applied to the various digital and analog devices. Table 21 is a summary of the infrared scans conducted. In most instances, the temperature gradient plots were made for each type of device in both orientations. Note, however, that because of the special device mounting methods employed during thermal mapping in this study, the data in Table 21 should not be directly compared to any other Θ_{js} beam lead device data.

Temperatures were recorded under nominal voltage operating conditions, but a complete temperature survey of the device was not made if a significant gradient was not observed; voltage was then increased and a complete scan conducted. An oscilloscope display of the device output was used to verify correct operation. The thermal resistance, Θ_{js}, cited in the table was from junction to substrate, and was calculated as follows:

$$\Theta_{js} = \frac{T_{(\text{device hot spot})} - T_{(\text{substrate hot spot})}}{\text{Power}}$$

where:

Θ_{js} = thermal resistance from the hottest spot to the substrate

T = temperature

The right hand column in the following table indicates which devices were plotted in detail and their corresponding figure number. All devices tested were not plotted either due to device failures or due to insignificant temperature gradients in some nominal power cases. All pictures of the metallization are shown with the image reversed so that beam-lead connected (metallization down) devices will appear as seen from this back side. For readers familiar with the device layout and the equivalent circuit (component) design, Pin No. 1 is indicated on each figure (reference to Table 4).

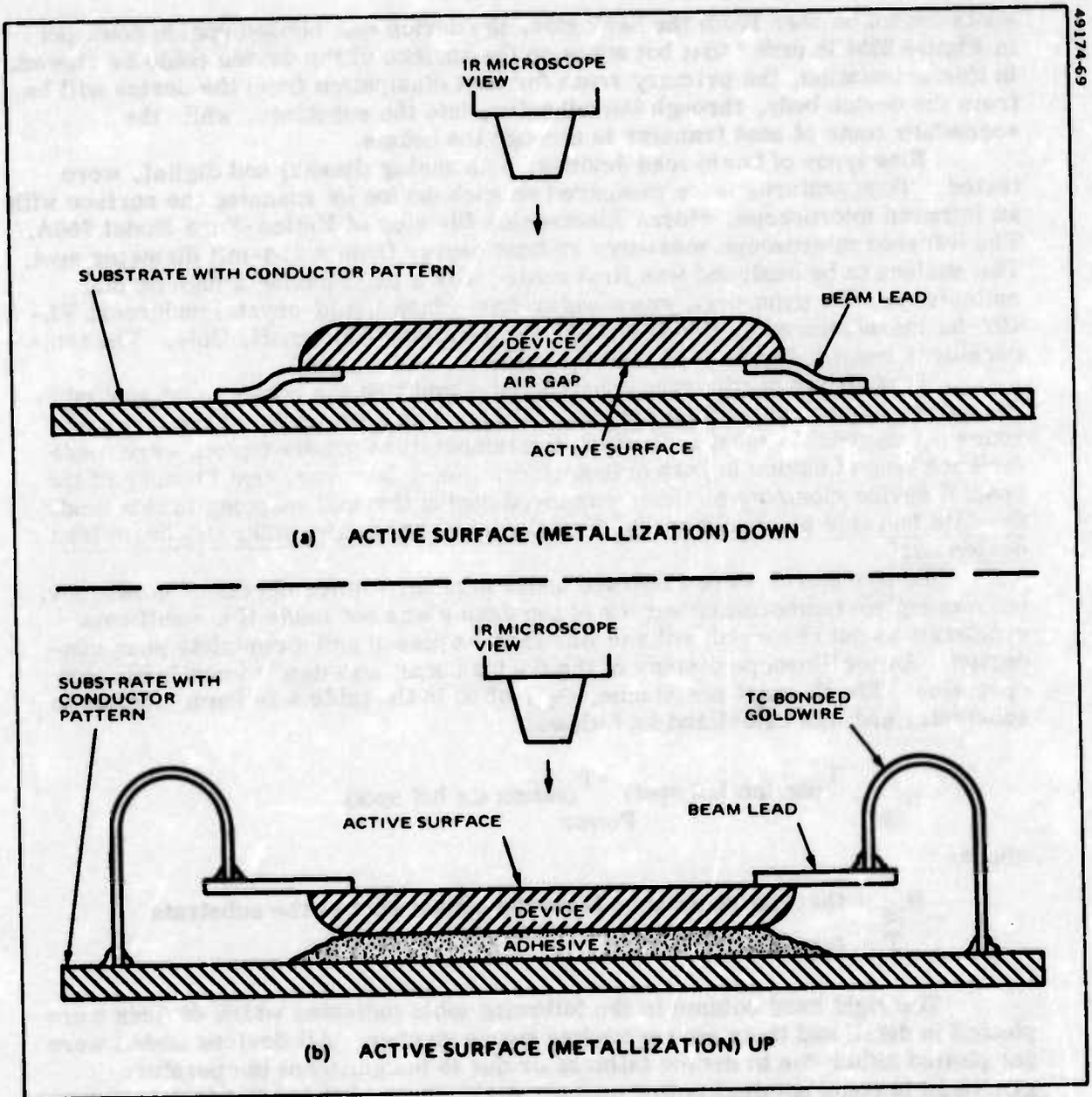


Figure 22. Two Orientations Used in Thermal Mapping Analysis. Metallization down is the normal orientation for mounting beam lead devices, but this does not present an active surface view for the IR microscope. Mounting with metallization up enabled hot spots on the device surface to be plotted.

TABLE 21. SUMMARY OF INFRARED SCANNING OF BEAM LEAD DEVICES

Device	Serial No.	T_{max} (°C)	$T_{subst.}$ (°C)	Voltage (V)	Power (mW)	θ_{js} (°C/W)[1]	Mounting[2]	Figure No.
SC148	-	38.5	29.5	+ 5 nom	119	76	up	not plotted
	1	86	53.5	+ 8	418	77	up	23
	-	36	29	+ 5 nom	140	50	down	not plotted
	2	67.5	50	+ 8	381	46	down	24
SC149	1	38.5	29	+ 5 nom	102	93	up	25
	1	72.5	42	+ 8	305	100	up	26
	-	33	28.5	+ 5 nom	99	45	down	not plotted
	-	71.5	52	+ 8	389	50	down	not plotted
	1	36.5	29	+ 5 nom	53	141	up	not plotted
SC150	1	50	35[3]		105[3]	145	up	27
	1	69	44.5	+ 8.5	181	135	up	not plotted
	1	75	47[3]		205[3]	140	up	28
	2	48	30	+10	212	85	down	29
SC151	-	25	-	+ 5 nom	33	-	down	not plotted
	1	41	28.5	+ 9.6	125	100	down	30
SC152	-	31.5	25.5	+15 -15 nom	75	80	down	not plotted
	1	40	29.5	+20 -20	124	85	down	31
SC153	-	-	-	+15 -15 nom	63	-	up	not plotted
	1	44	28[3]	+20 -20	106	151	up	32
	3	-	-	+15 -15 nom	72	-	down	not plotted
	2	37.5	28.5	+18 -18	122	74	down	33

7. RESULTS OF THE THERMAL MAPPING ANALYSIS (Continued)

TABLE 21. SUMMARY OF INFRARED SCANNING OF BEAM LEAD DEVICES (Continued)

Device	Serial No.	T_{max} (°C)	$T_{subst.}$ (°C)	Voltage (V)	Power (mW)	Θ_{js} (1) (°C/W)	Mounting (2)	Figure No.
SC154	3	34	25 (3)	+15 -15 nom	62	146	up	34
	2	28	-	-15 -15 nom	69	-	down	not plotted
	2	30.5	27 (3)	+17 -17	85	41	down	not plotted
	4	77	51.5	+29 -33	552	46	down	35
SC155	1	-	-	+15 -15 nom	60	-	down	not plotted
	1	32.5	28	+30 -30	120	38	down	36
	2	36.5	30	+30 -30	138	47	down	37
SC156	1	107	25	- 6 +12 nom	122	673	up (4)	38
	2	42	29 (3)	- 6 +12	171	76	up	39
	2	77	43	- 8 -15	391	84	up	40
	2	107	57.5	-10 +17	574	86	up	41
	4	34.5	27	- 6 +12 nom	103	74	down	42
	4	49	34	- 8 +15	192	78	down	43
	4	85.5	52.5	-12 +20	469	70	down	44

(1) Θ_{js} is device hot spot-to-substrate thermal resistance. This Θ_{js} should not be compared with other Θ_{js} for beam lead devices because of the special nature of the bonding methods employed (see Figure 22).

(2) up – mounted with metallization facing upward, and with Ablefilm 517 adhesive, 3 mils thick

(3) Estimated value

(4) Mounted on plastic microdot.

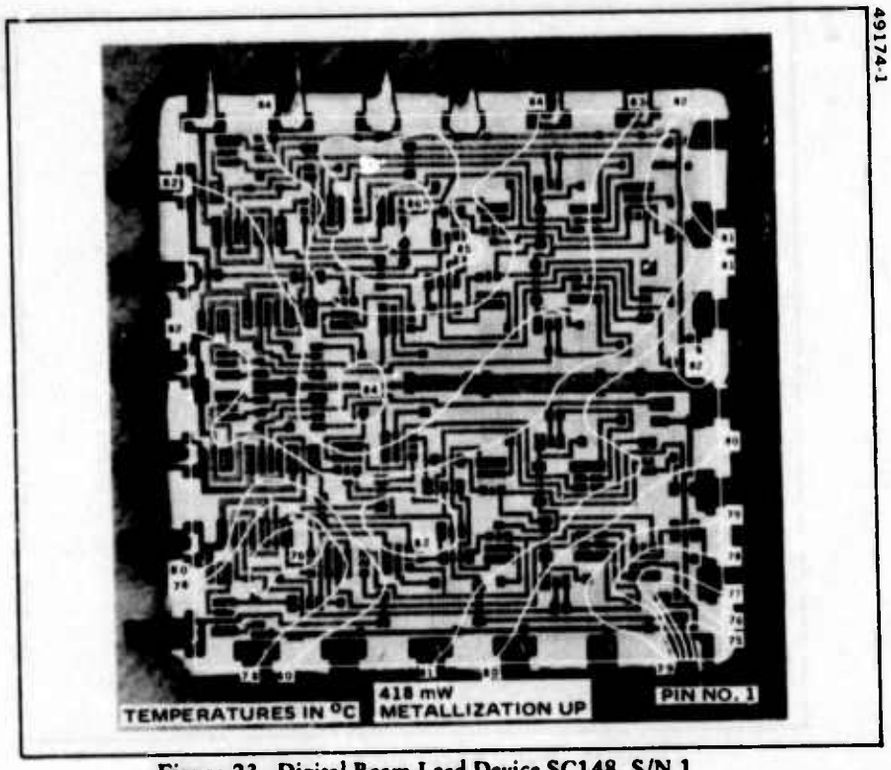


Figure 23. Digital Beam Lead Device SC148, S/N 1

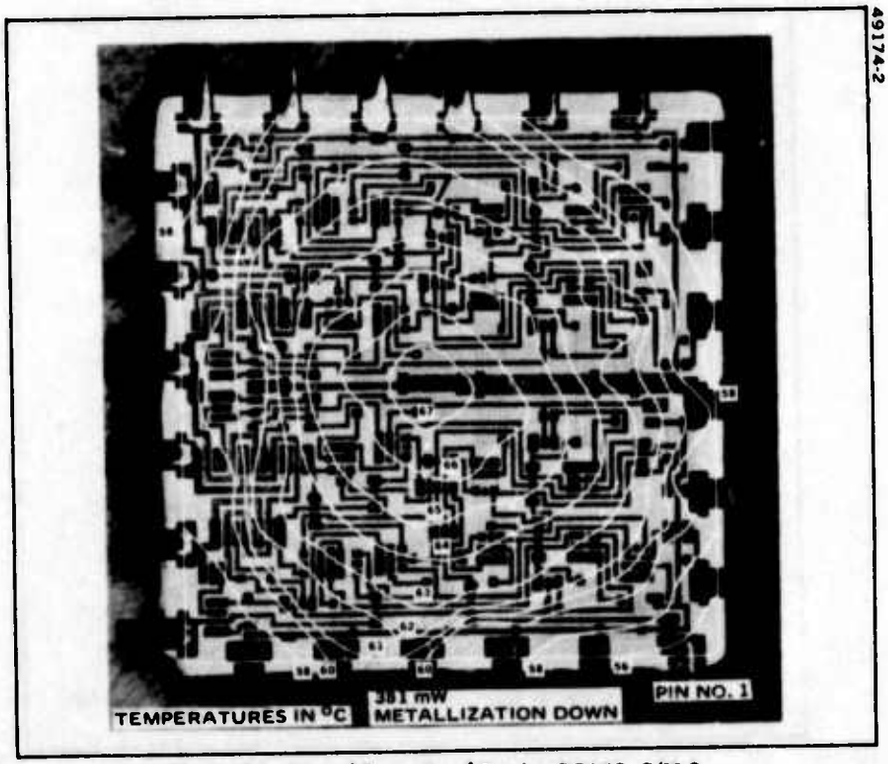


Figure 24. Digital Beam Lead Device SC148, S/N 2

Figure 23 shows typical temperature distribution with high power. Failure of diodes in the vicinity of the 86° region (in upper center) has been observed. Hot spots in Figure 24 generally cannot be observed due to the heat spreading effect of the thick silicon material. (Compare with Figure 23.)

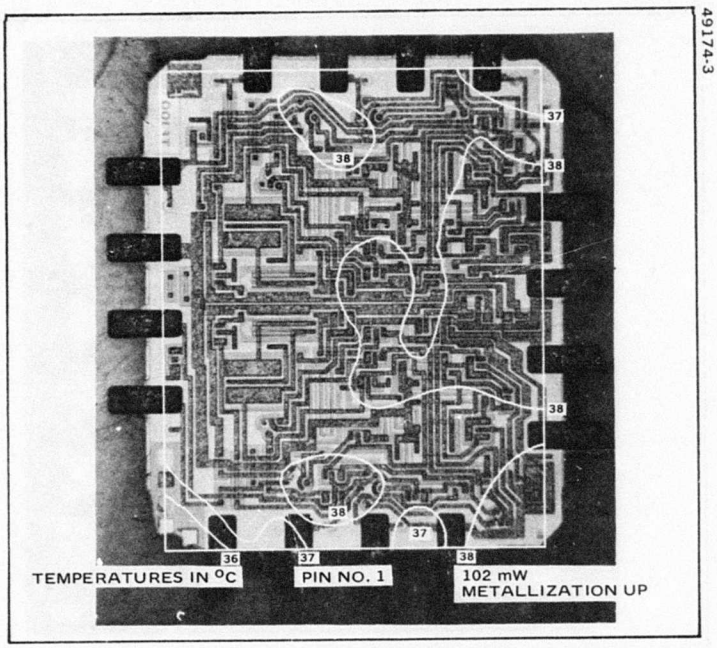


Figure 25. Digital Beam Lead Device SC149, S/N 1

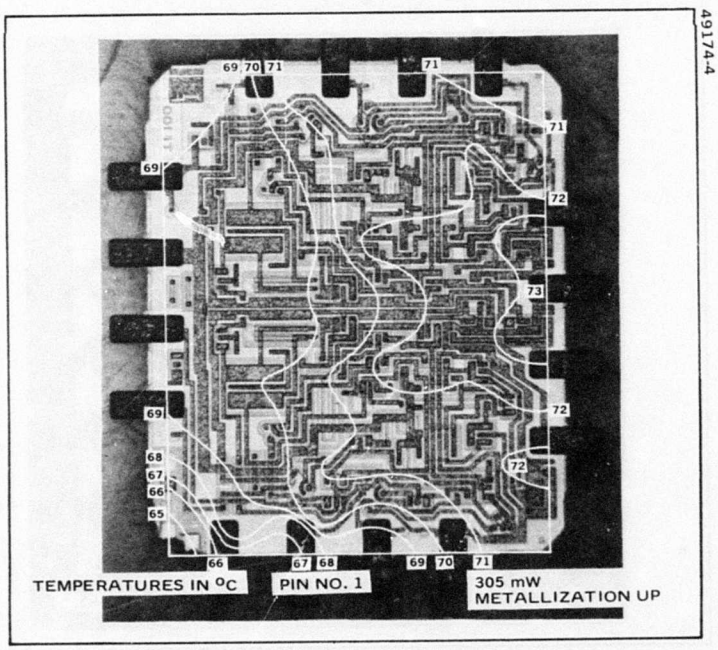


Figure 26. Digital Beam Lead Device SC149, S/N 1

As expected, the power density appears to increase on the right hand side of the device as the dissipated power increases.

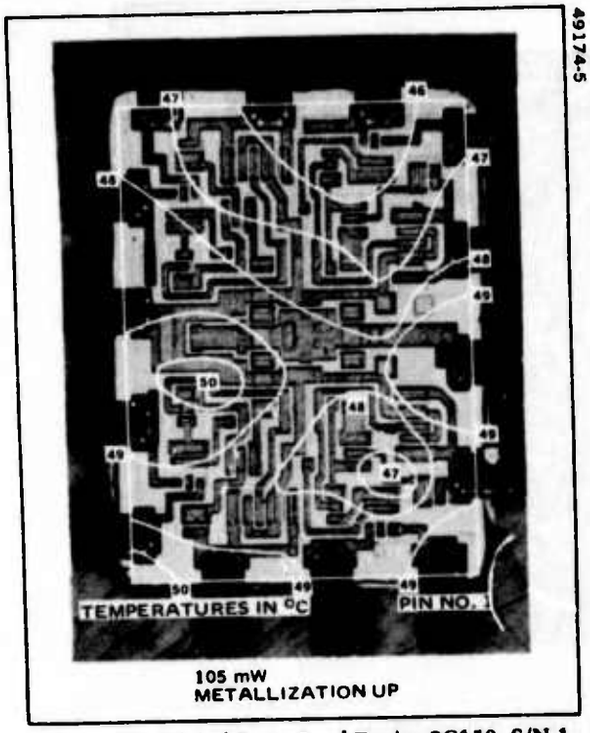


Figure 27. Digital Beam Lead Device SC150, S/N 1

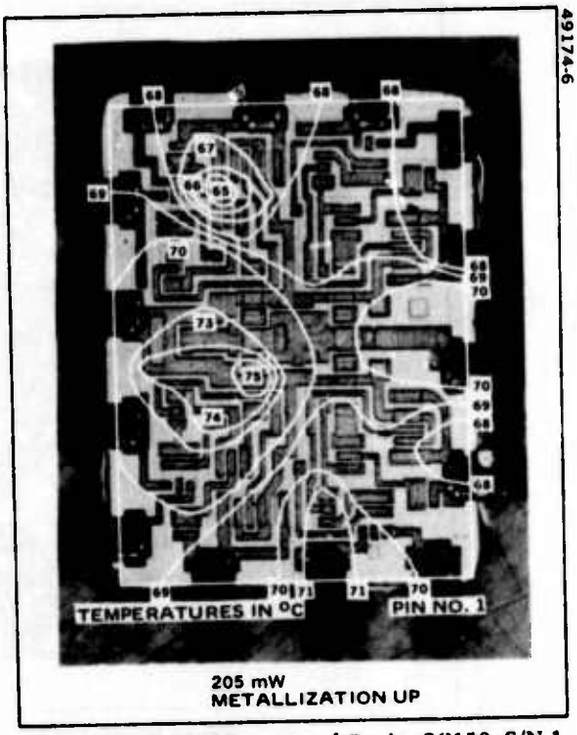


Figure 28. Digital Beam Lead Device SC150, S/N 1

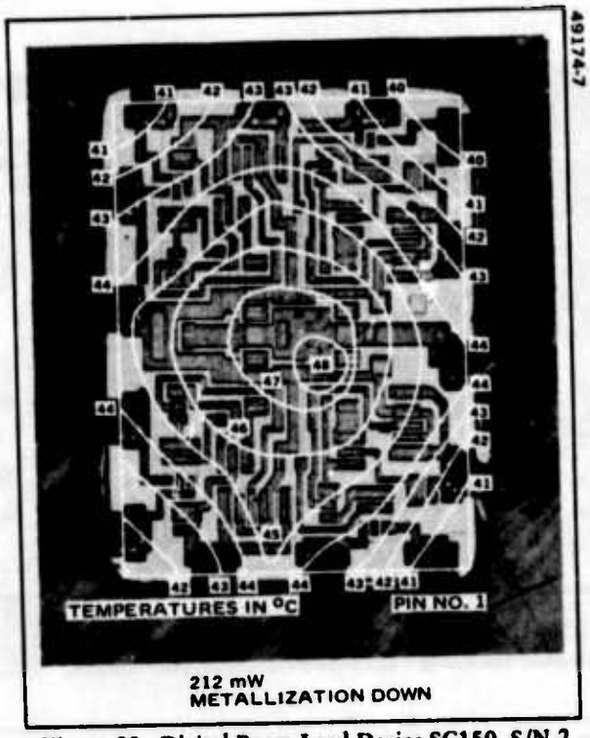


Figure 29. Digital Beam Lead Device SC150, S/N 2

The data shown for Figures 27 and 28 demands further analysis. For instance, Figure 28 shows a hot spot developing (with an increase in power) near left-center of device, while a "cold" spot is developing in upper left area. Figure 29 shows the expected temperature distribution of a device so mounted.

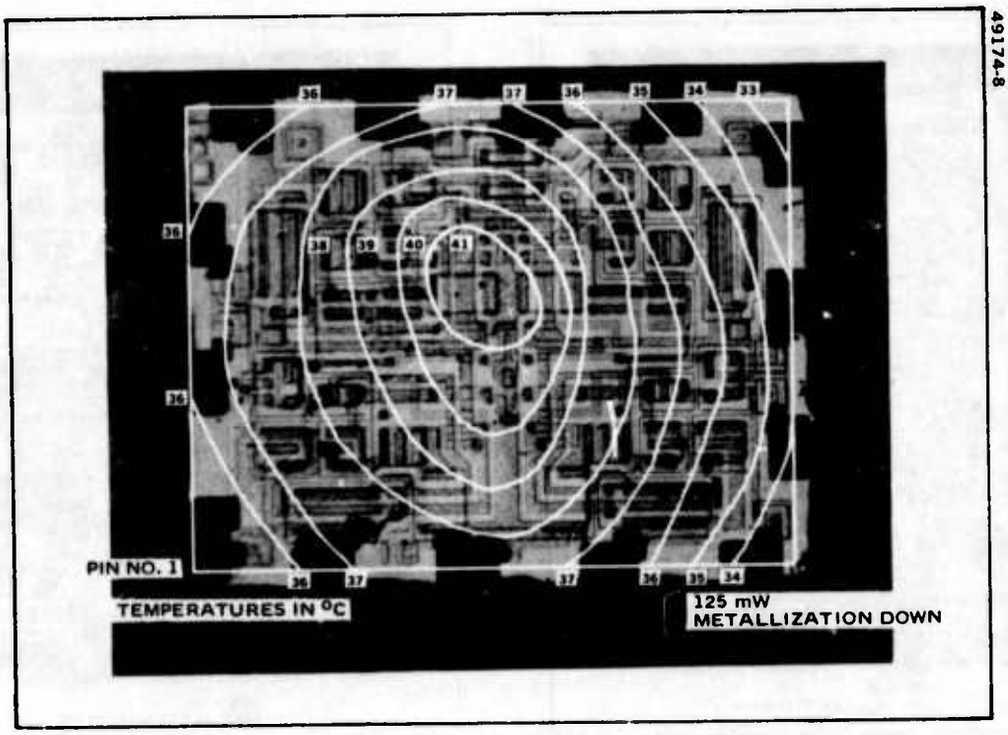


Figure 30. Digital Beam Lead Device SC151, S/N 1

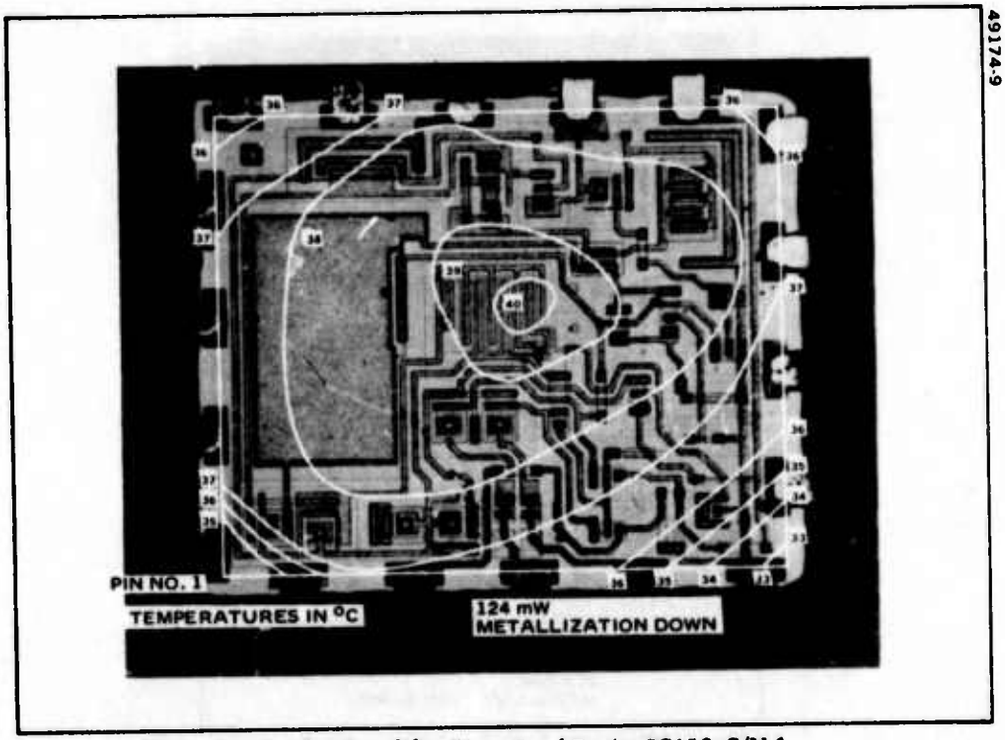


Figure 31. Analog Amplifier Beam Lead Device SC152, S/N 1

This figure shows the expected temperature distribution for these conditions. Note the gradients in lower corners and the relatively uniform temperature over most of the surface area.

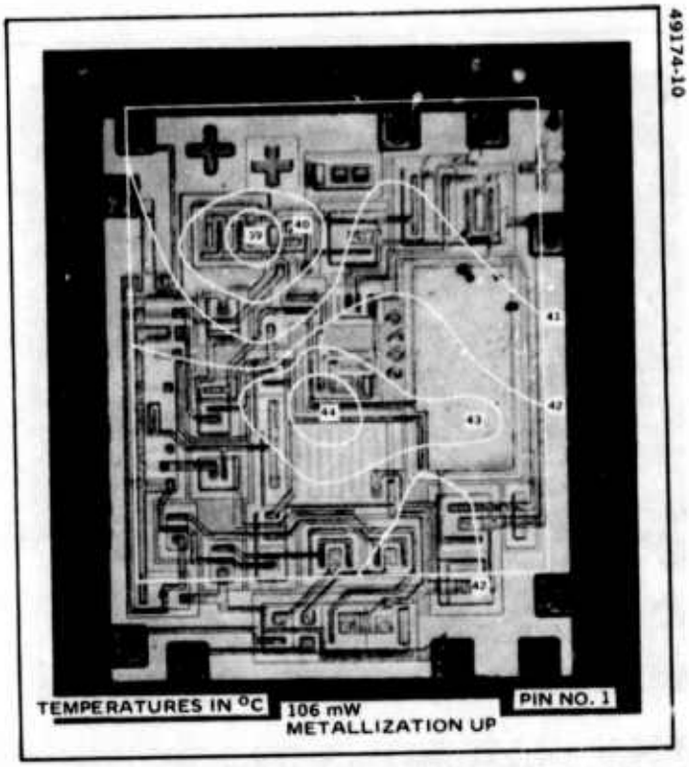


Figure 32. Analog Amplifier Beam Lead Device SC153, S/N 1

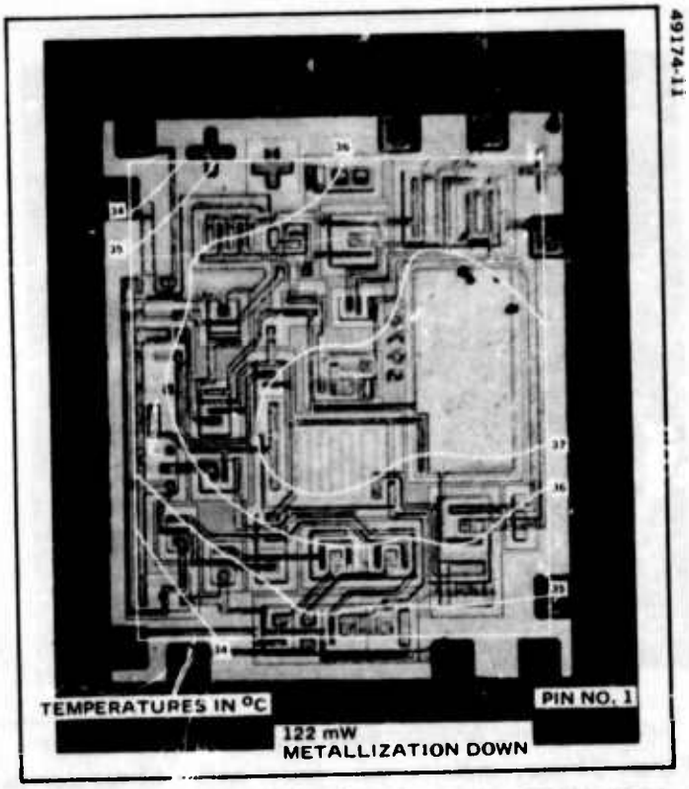


Figure 33. Analog Amplifier Beam Lead Device SC153, S/N 2

As expected, a warm area is indicated over the resistor in the center of the device in Figure 32. In Figure 33, only 3°C temperature range for the entire device is noted.

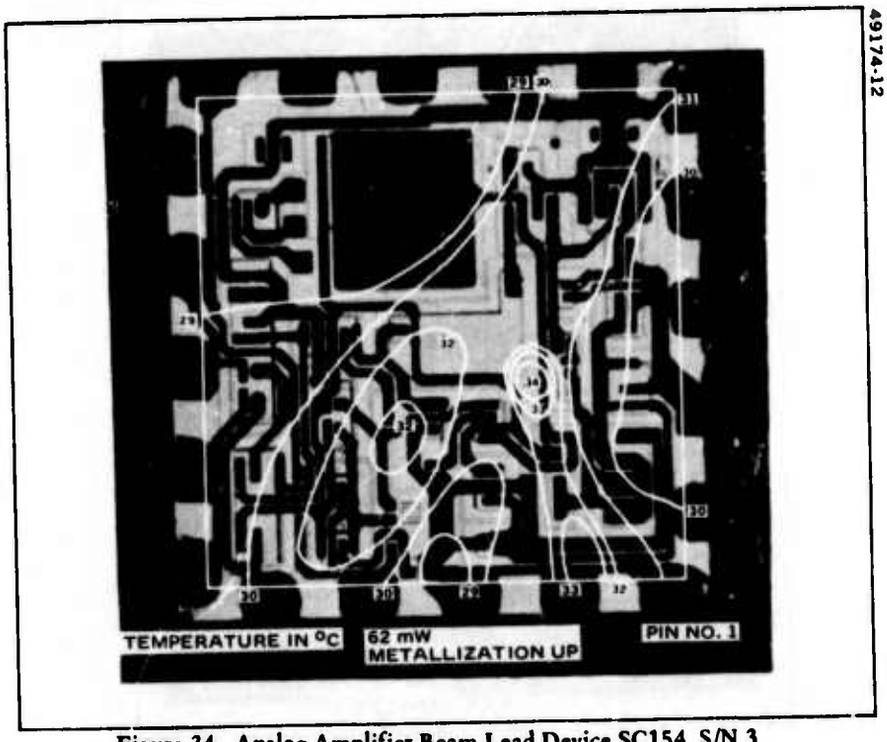


Figure 34. Analog Amplifier Beam Lead Device SC154, S/N 3

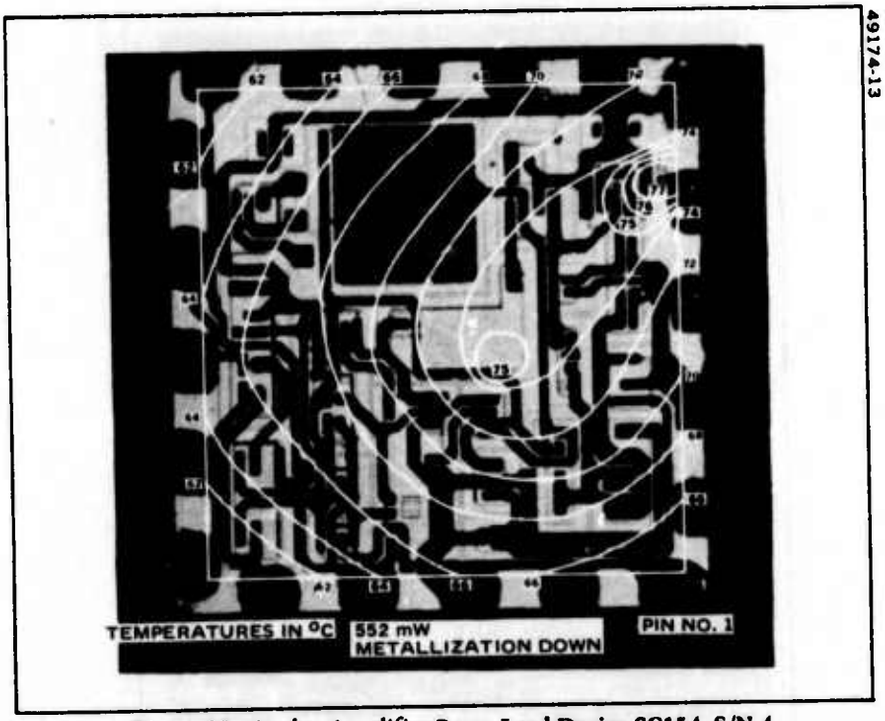


Figure 35. Analog Amplifier Beam Lead Device SC154, S/N 4

The hot spot in Figure 34 may indicate poor termination of resistor in center area. The device in Figure 35 had failed at lower power and no output waveform was present on the oscilloscope. Hot spot in upper right may indicate a poor termination to a beam lead. (A hot spot is also present near the resistor noted on the S/N 3 device shown in Figure 34.)

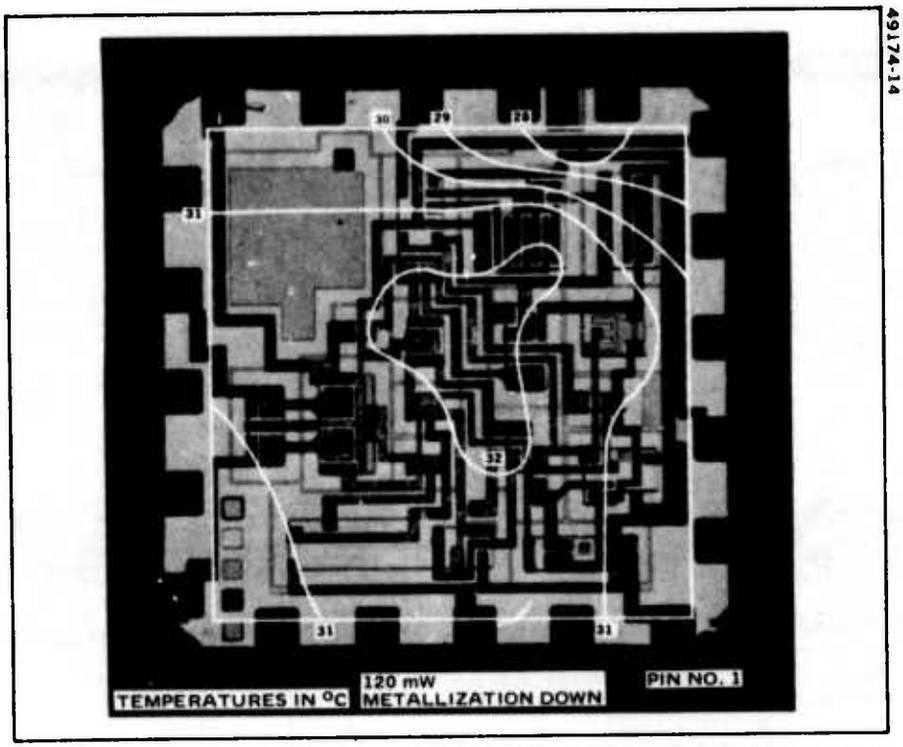


Figure 36. Analog Amplifier Beam Lead Device SC155, S/N 1

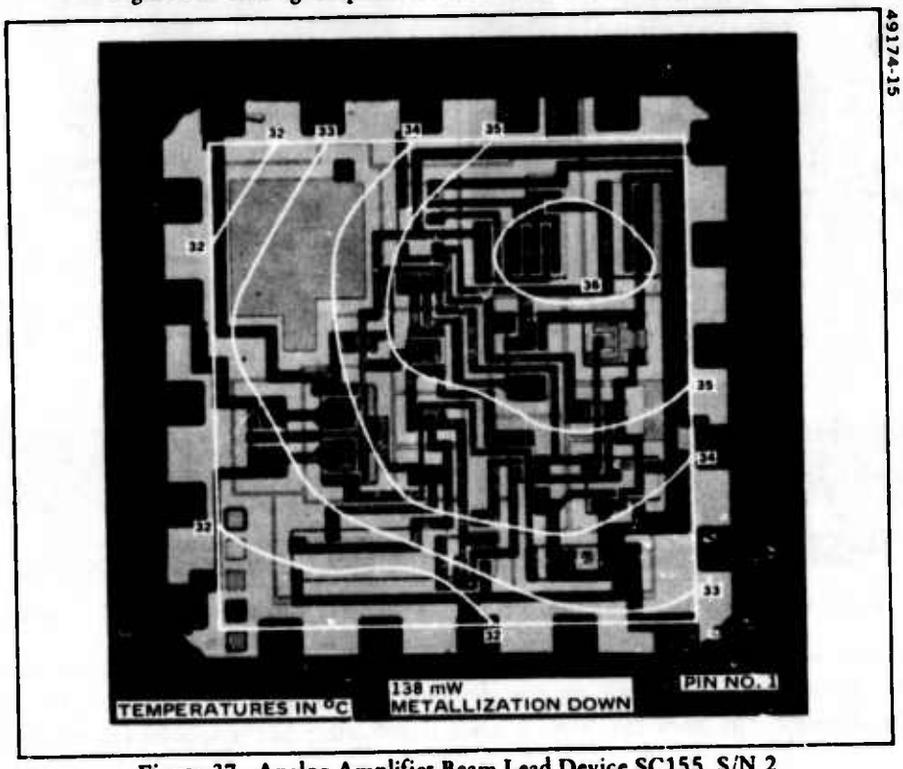


Figure 37. Analog Amplifier Beam Lead Device SC155, S/N 2

In Fiure 36, only a 40°C gradient noted. Figure 37 is another instance of data needing further analysis. Comparing Figure 37 (S/N 2) with Figure 36 (S/N 2), it is noted that both devices were mounted in the same manner and under similar voltage conditions. Both devices have a 4°C gradient but S/N 2 indicates more heat concentrated near the output transistor in the upper right, and draws more power.

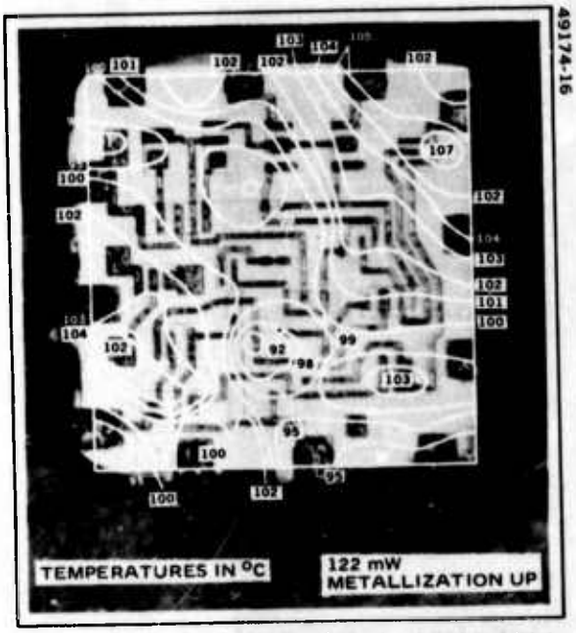


Figure 38. Analog Beam Lead Device SC156, S/N 1. (This device was mounted on a plastic microdot.)

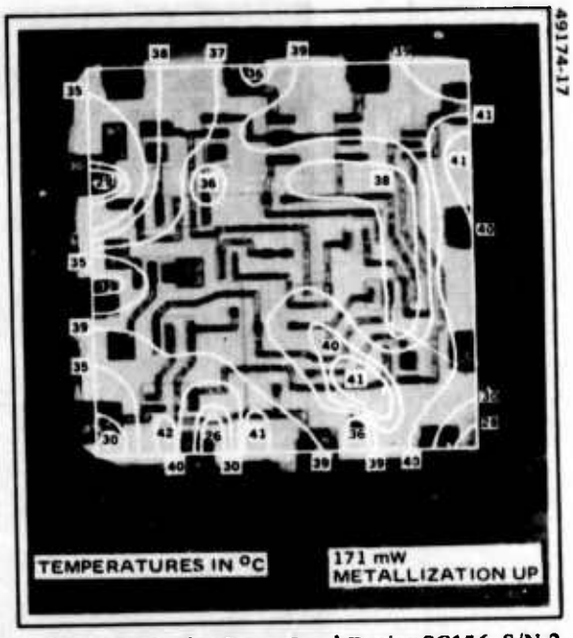


Figure 39. Analog Beam Lead Device SC156, S/N 2

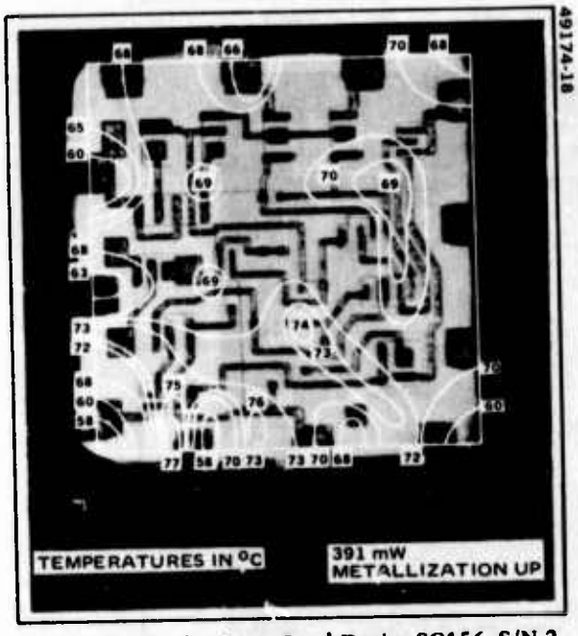


Figure 40. Analog Beam Lead Device SC156, S/N 2

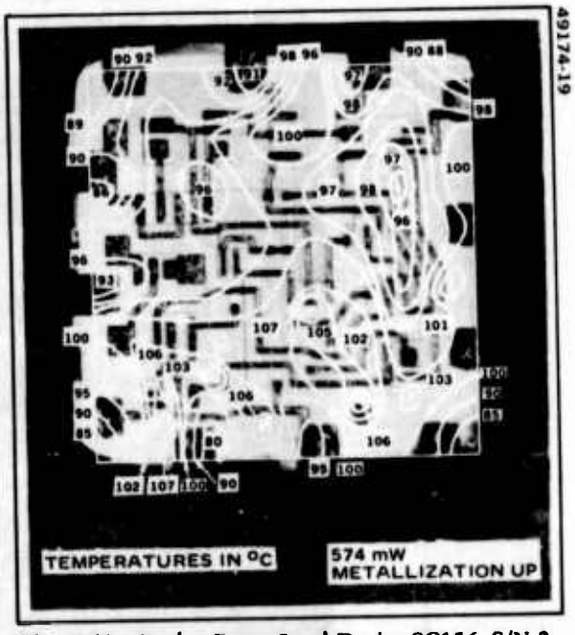


Figure 41. Analog Beam Lead Device SC156, S/N 2

High temperature is noted in Figure 38 with relatively low power due to poor heat sinking to the substrate. (Heat sinks apparent on the device indicate spot contact with the plastic microdot under the device). In data for S/N 2, note developing hot spots in lower right.

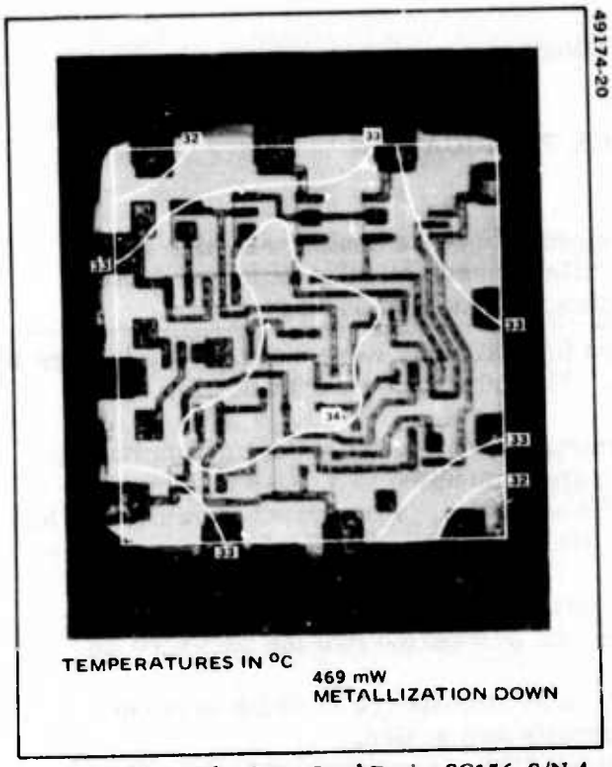


Figure 42. Analog Beam Lead Device SC156, S/N 4

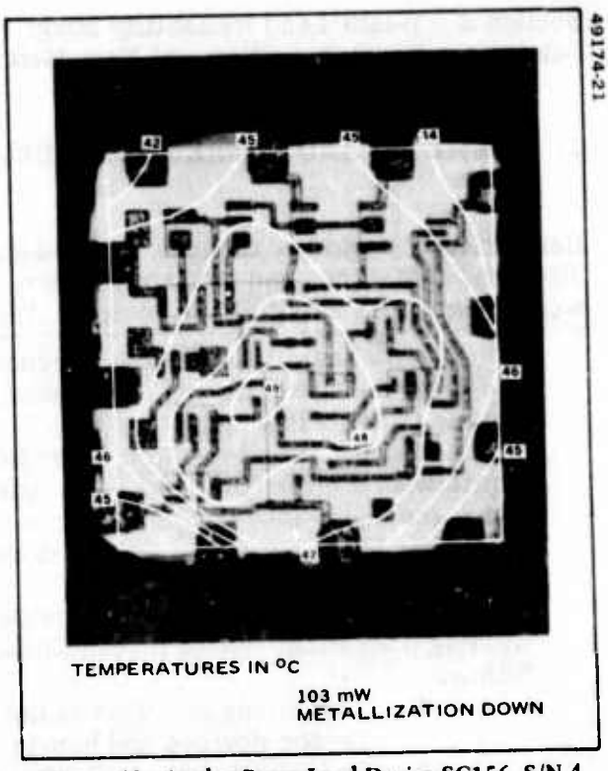


Figure 43. Analog Beam Lead Device SC156, S/N 4

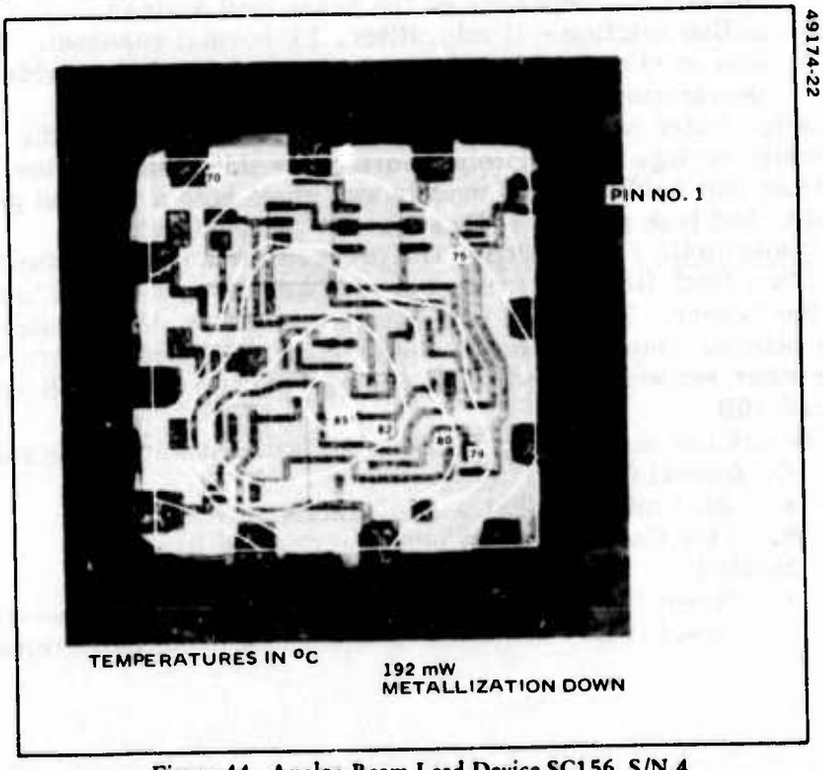


Figure 44. Analog Beam Lead Device SC156, S/N 4

Note increasing gradients due to increased power. Figure 42 shows that a plot can be constructed even though only 2°C gradient occurs.

Section 2 – Beam Lead Reliability Study
Subsection B – Fabrication and Test Methodology

1. HERMETIC AND NONHERMETIC DEVICE FABRICATION

Hermetically packaged devices were subgrouped into those sealed with high purity nitrogen, moisture, and salt atmosphere, while nonhermetically packaged devices were subgrouped using either conformal coatings or molded packages.

The beam lead devices purchased for the study were packaged by Hughes in two groups: hermetic and nonhermetic. The fabrication variations for both groups is described below.

Hermetic Fabrication – The hermetic module consists of an alumina substrate with a thick film gold conductor pattern mounted to a TO-8 header, to which the beam lead device was then wobble bonded. Finally, as shown in the left of Figure 45, the cap was welded to the TO-8 header. The final construction is shown in Figure 46A.

The hermetic group was divided into three subgroups. During the cap welding operation, one of three atmospheres was sealed into the packages as follows:

1. Dry nitrogen – This is the normal atmosphere in which semiconductor devices and hybrid circuits are sealed.
2. Deionized water – (1 microliter) Water was included to determine the effect of moisture on the beam lead devices.
3. Saline solution – (1 microliter, 1% normal solution). This solution was used both to test device hermeticity and to provide a sodium ion penetration test.

The deionized water and the saline solution were metered into the TO-8 cap with a hypodermic syringe immediately before cap welding each device.

After cap welding, each module was given both a fine and gross leak test. All modules had leak rates less than 1×10^{-7} atm-cc/second.

Nonhermetic Fabrication – The process for a nonhermetic device also started with a thick film substrate, but pins were then soldered to the substrate to make the header. The beam lead device was then wobble bonded to the substrate as before. One set of nonhermetic assemblies was conformally coated, while the other set was molded. The package construction is also shown in Figures 45 and 46B.

The devices in the nonhermetic group were subdivided as follows:

- Conformal Coat
  a. 3M Scotchcast 281 A & B Electrical Resin.
  b. Dow Corning 62-047 Junction Coating Resin.
- Molded
  a. Hysol C-59 Encapsulating System (with mold release).
  b. Hysol C-59 Encapsulating System (without mold release).

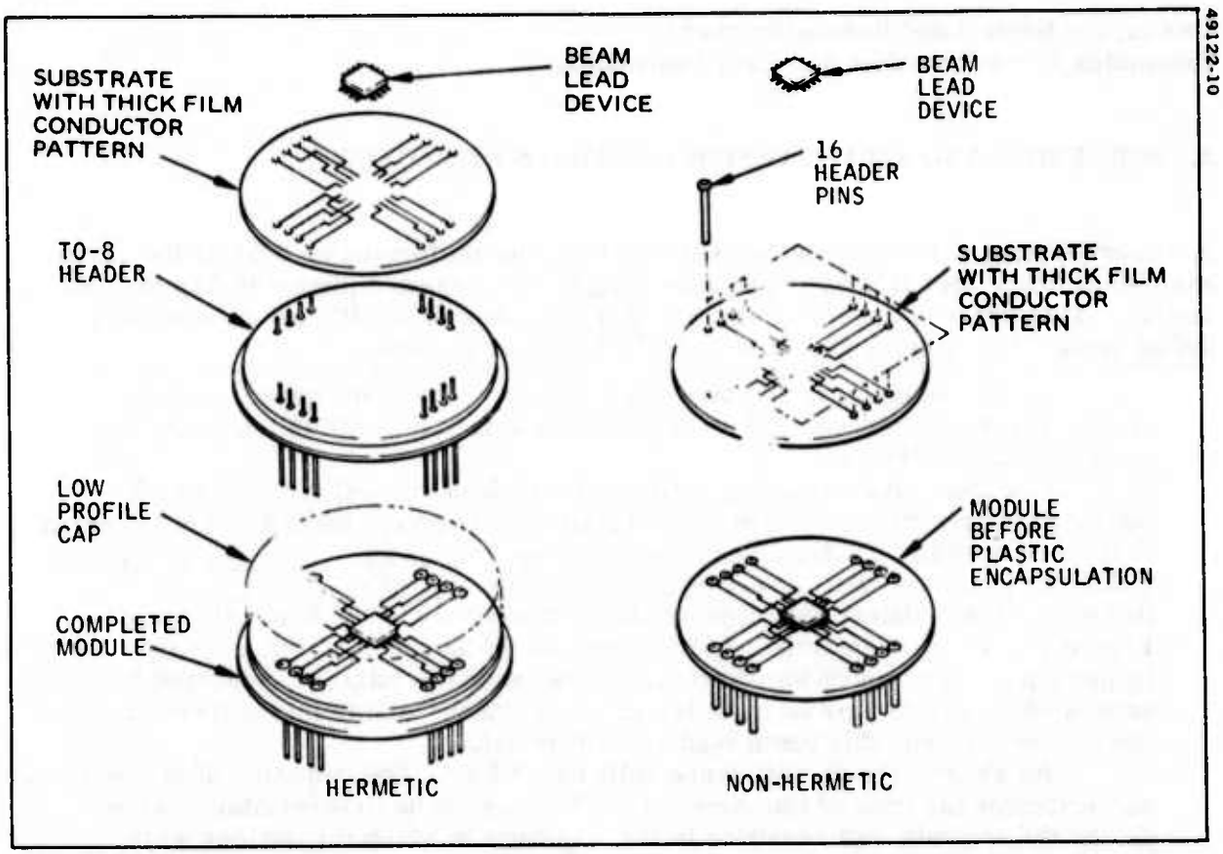


Figure 45. Exploded View of Package Construction. The hermetic devices were cap welded, while one of the non-hermetic devices was conformally coated and the other group molded.

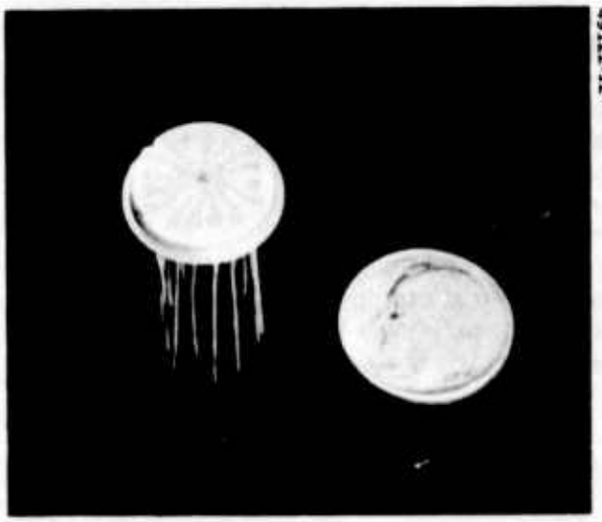


Figure 46A. Hermetic Beam Lead Module Package without Cap

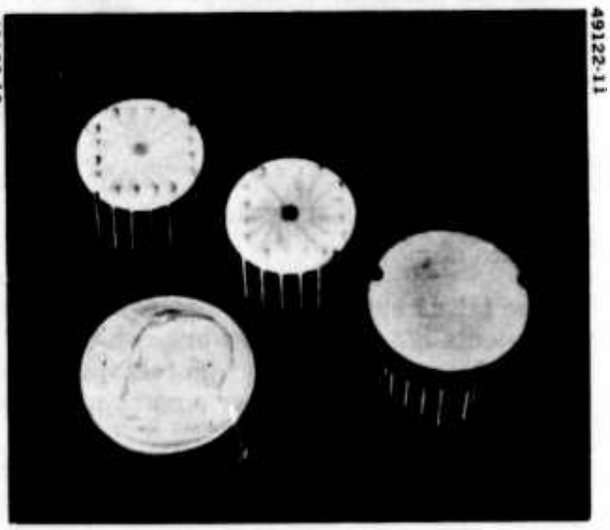


Figure 46B. Conformally Coated and Molded Non-Hermetic Beam Lead Module Packages

2. SCREENING AND STRESS TESTING METHODS EMPLOYED

A comprehensive screening and step stress test was performed on 3456 of the device samples in three lots (1152 per lot) according to the sequence prescribed in the test matrix. This approach provided the maximum number of conditions to accurately define design deficiencies and associated failure mechanisms.

At the beginning of the program, a major cause for concern was the ability of various screens and stress tests to induce failures in the beam lead sealed junction devices.

For example, assuming available beam lead reliability data, which indicated failure rates of 0.005%/1000 hours, is correct, extrapolation indicated that acceleration factors must be 10^6 times in order to ensure at least 8 failures out of the chosen cell size at 16 samples per cell. However, it was determined that by using the stress tests scheme shown in Figure 47, an adequate number of failures would be provided for analysis. As it turned out, this concern was unwarranted because the failures generated from the screen/stress tests proved to be far in excess of those anticipated from predictions based on available beam lead reliability data.

As shown, the devices were split into 3 lots. The sequence of stress tests was different for each of the three lots. This was done to determine whether device failure rate was sensitive to the sequence in which the devices were stressed.

The actual stress test conditions are shown in Figure 48. Note that before device assembly, all devices were 100% visually inspected to determine any visual anomalies which might later result in device failures. After assembly, all devices were 100% electrically tested to the following parameters:

- Analog Devices – (a) gain
  (b) bandwidth
  (c) linearity
  (d) off-set.
- Digital Devices – (a) input transistor levels
  (b) high and low output levels.

After devices from the screens or stress tests were automatically tested, the failed units were again tested on "bench set-ups" to confirm the failures. Rejects not confirmed were returned to the screen/stress tests sequence. The bench test was a go/no-go test and essentially only catastrophic failures were eliminated from further screening/stress testing.

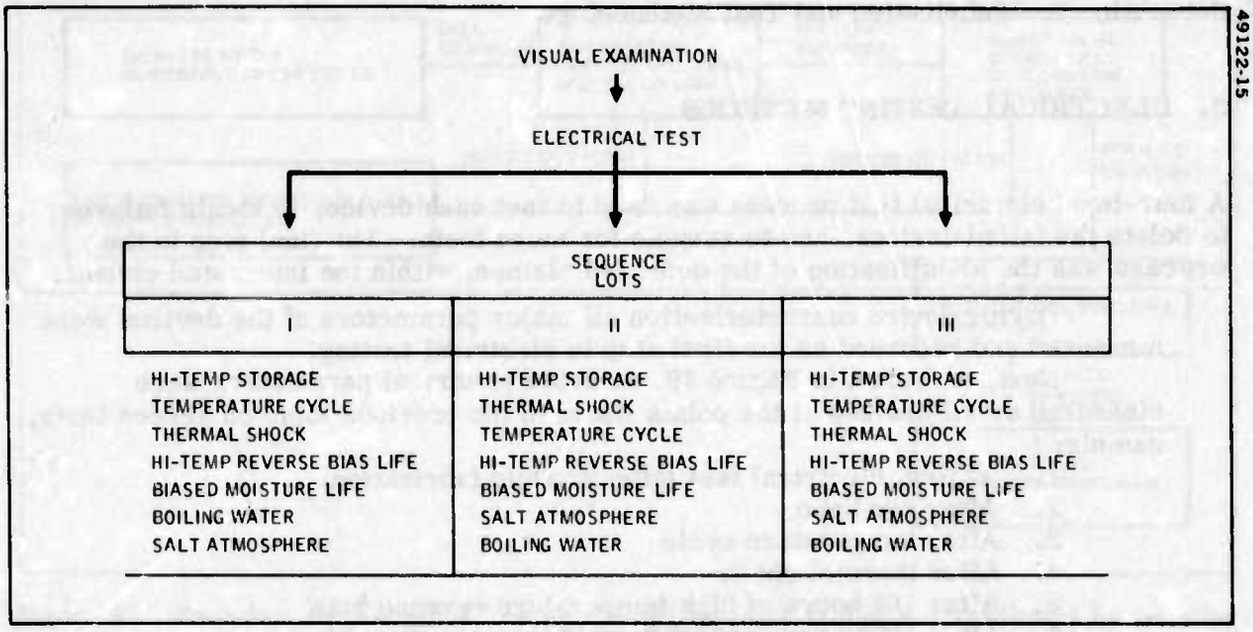


Figure 47. Stress Test Sequence

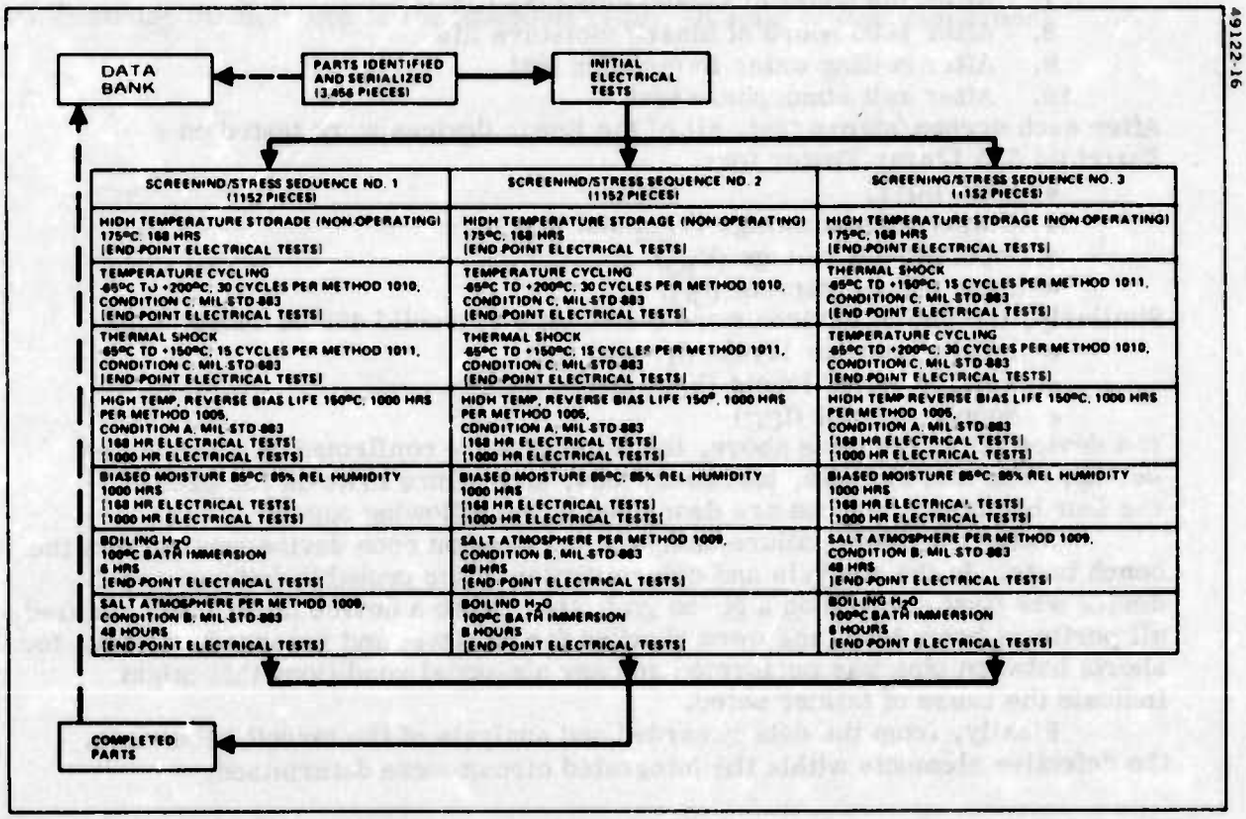


Figure 48. Detailed Stress Conditions Used in Screening Three Lots. This sequence was chosen to provide highest device fall-out in an optimum manner. Note that the first 3 screens are "lot" type static tests while the next two tests are dynamic tests done on each device. The last three tests were aimed at determining the "moisture coating" integrity of the devices. Subsequent evaluation showed that changing the test sequence had no significant different in impact on test results.

3. ELECTRICAL TESTING METHODS

A four-level electrical test process was used to test each device, to locate failures, to delete the failed devices, and to recycle for more tests. The final step in the process was the identification of the defective element within the integrated circuit.

During device characterization all major parameters of the devices were measured and recorded as the first step in electrical testing.

Next, as shown in Figure 49, selected electrical parameters were measured on all devices at the points listed in the previous topic on screen tests, namely:

1. At first electrical test (after module fabrication)
2. After age bake
3. After temperature cycle
4. After thermal shock
5. After 168 hours of high temperature reverse bias
6. After 1000 hours of high temperature reverse bias
7. After 168 hours of biased moisture life
8. After 1000 hours of biased moisture life
9. After boiling water immersion test
10. After salt atmosphere test

After each screen/stress test, all of the linear devices were tested on a Fairchild 335 Linear Tester for:

- Gain (A_{OL})
- Output voltage swings (V_{OH} and V_{OL})
- Input off-set voltage (V_{IO})
- Input off-set current (I_{IO})

Similarly, the digital devices were tested on a Fairchild 4000M Tester for:

- Input transistor levels (I_{IL} and I_{IH})
- Voltage output levels (V_{OH} and V_{OL})
- Supply current (I_{CC})

If a device failed the tests above, the failures were confirmed on a bench test set-up. The test circuits, test conditions, and failure criteria for each of the four basic device types are described in the following pages.

Next, pin-to-pin failure analysis was done on each device routed from the bench tests. In the analysis and determination of the probable failures, each device was first checked on a go-no go basis. When a device failure was verified, all pertinent beam lead pins were checked for DC level and recorded. Checks for shorts between pins was performed and any abnormal conditions that might indicate the cause of failure noted.

Finally, from the data recorded and analysis of the circuit schematic, the defective elements within the integrated circuit were determined.

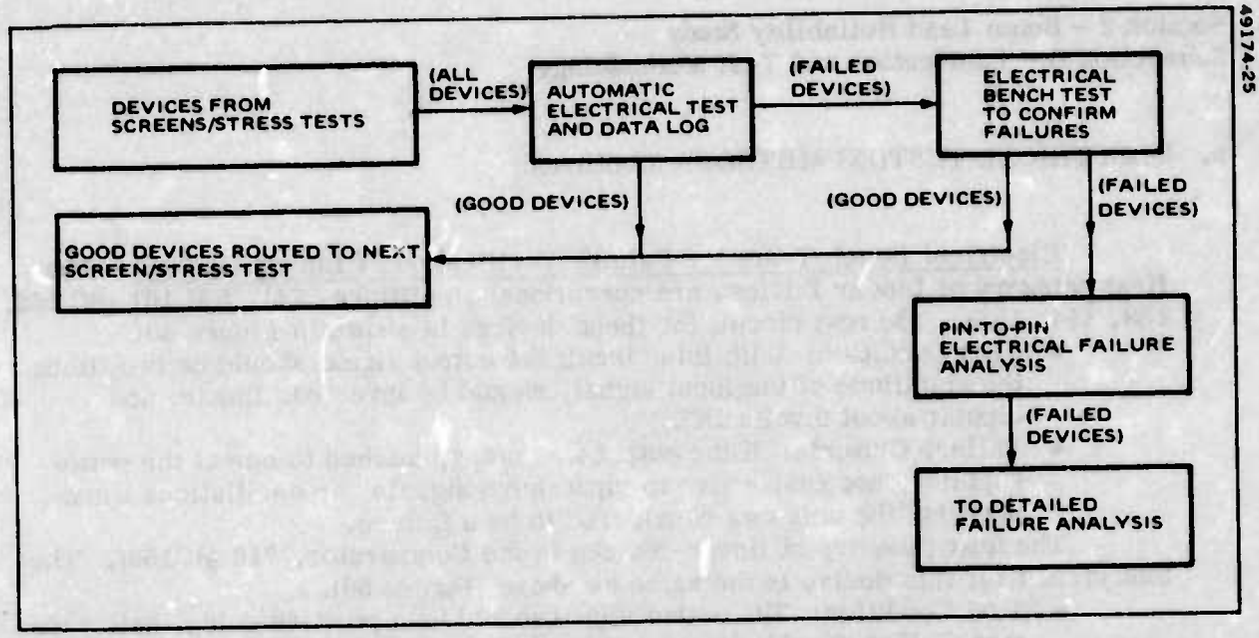


Figure 49. Procedure for Electrical Testing. Note that each failure was confirmed by retesting on a bench test setup. Pin-to-pin electrical failure analysis was done on all confirmed failures to determine the next step in the procedure (x-ray, IR scan, or de-encapsulation).

3. ELECTRICAL TESTING METHODS (Continued)

Electrical Bench Tests for Failure Verification of Linear Devices – The first category of Linear Devices are operational amplifiers, 741, RM 101 (SC 152, 153, 154, 155). The test circuit for these devices is shown in Figure 50.

- Test Condition: With this circuit the output signal should be two times the amplitude of the input signal, should be inverted, linear, and bipolar about 0 volts DC.
- Failure Criteria: If the output was noisy, latched to one of the power supplies, not responsive to input drive signals, or oscillations were present, the unit was considered to be a failure.

The next category of linear devices is the Comparator, 710 (SC156). The test circuit for this device is the same as above (Figure 50).

- Test Condition: The output signal should be a positive going, half wave signal, that should clip when it reaches a 5 volt amplitude. Examples of the wave forms are shown in Figure 51.
- Failure Criteria: If the comparator output did not produce these waveforms, or was latched in some mode, the device was considered to be a failure.

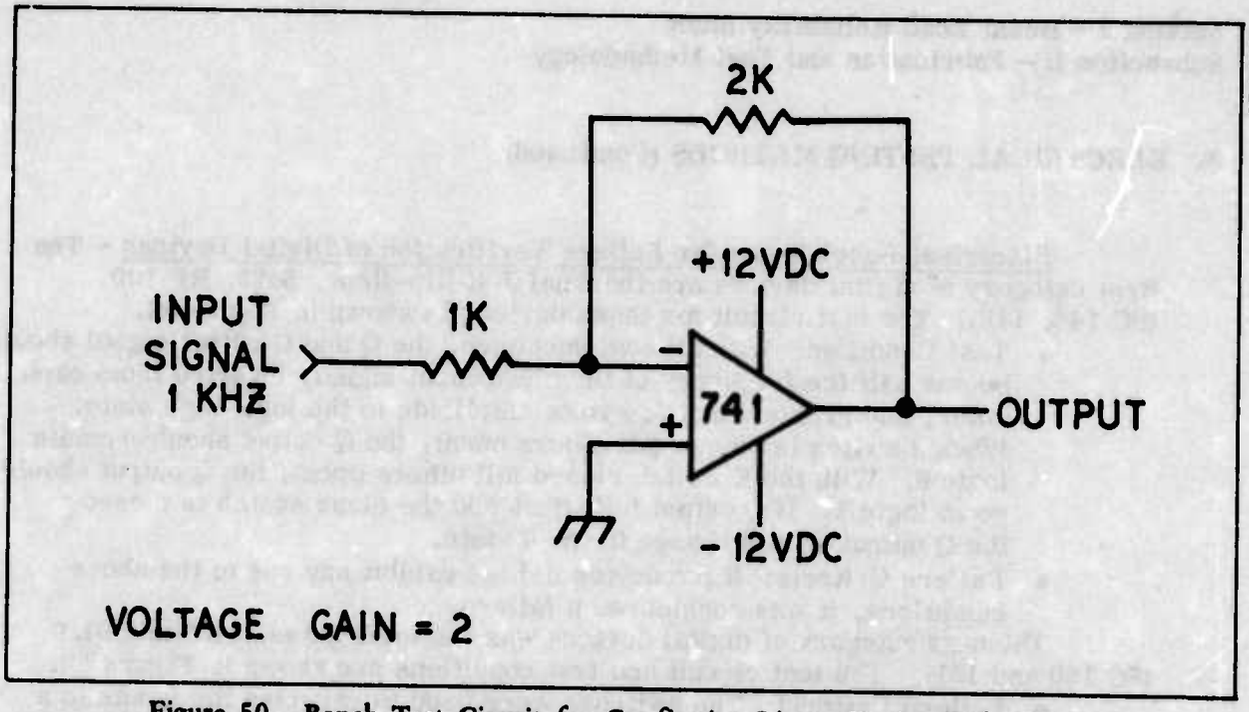


Figure 50. Bench Test Circuit for Confirming Linear Device Failures

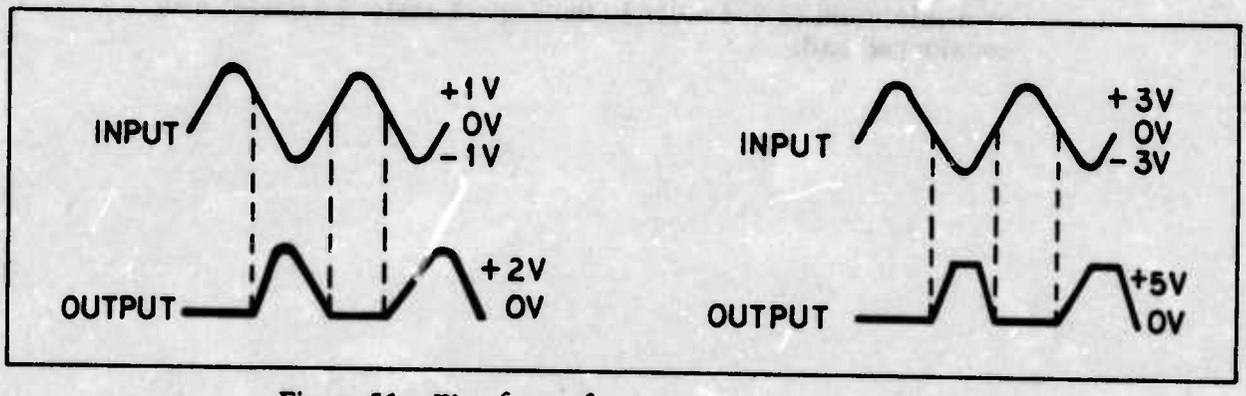


Figure 51. Waveforms for Linear Comparator Circuit

3. ELECTRICAL TESTING METHODS (Continued)

Electrical Bench Tests for Failure Verification of Digital Devices – The first category of digital devices are the Dual J-K flip-flops, 5473, RF 100 (SC 148, 149). The test circuit for these devices is shown in Figure 52.

- Test Condition: With all switches open, the Q and Q output signal should be one half the frequency of the clock input signal, inverted from each other, and greater than 2.4 volts amplitude in the logic high state. When J switch is closed (all others open), the Q output should remain logic 0. With the K switch closed (all others open), the Q output should go to logic 1. If Q output is logic 1 and the clear switch is closed the Q output should change to the 0 state.
- Failure Criteria: If the device did not exhibit any one of the above conditions, it was considered a failure.

The next category of digital devices was the logic gates, 5400 and 5410 (SC 150 and 151). The test circuit and test conditions are shown in Figure 53.

- Failure Criteria: The switches were used to exercise the inputs to a logic 1 or 0 condition. If any device failed to meet the above equations or a minimum of 2.4 volts in the logic 1 state the device was considered bad.

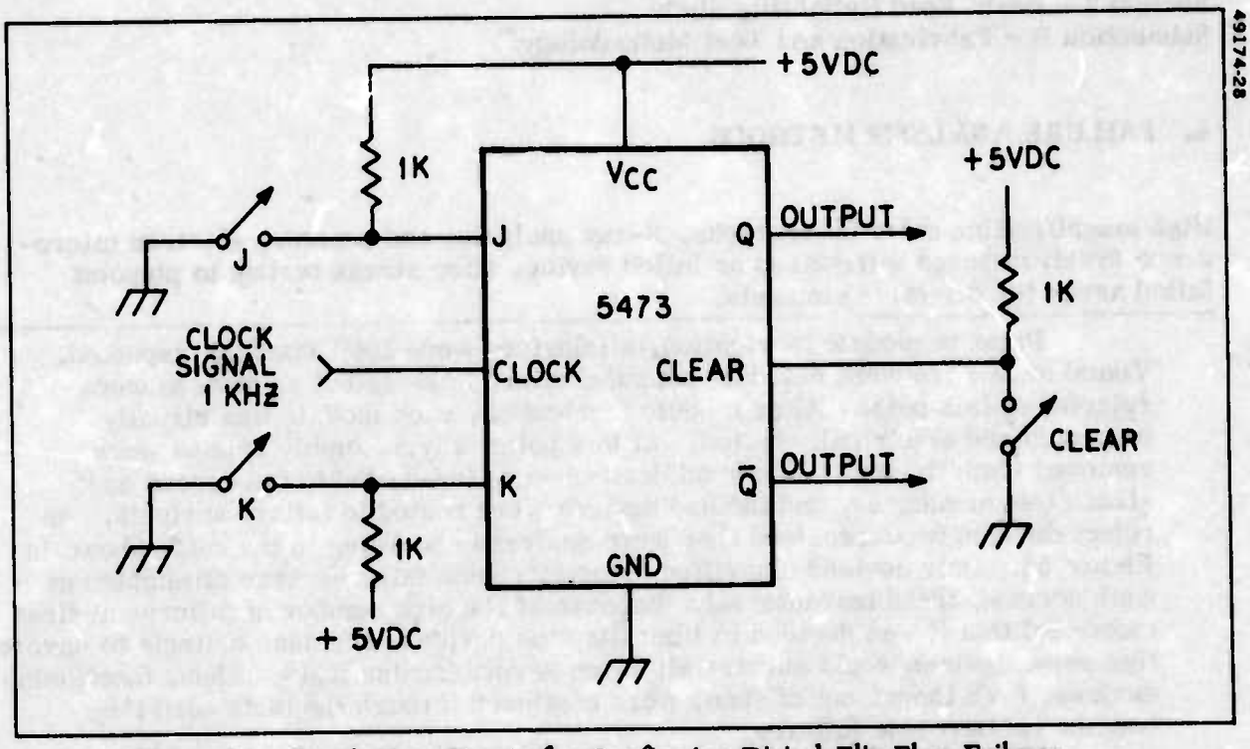


Figure 52. Bench Test Circuit for Confirming Digital Flip-Flop Failures

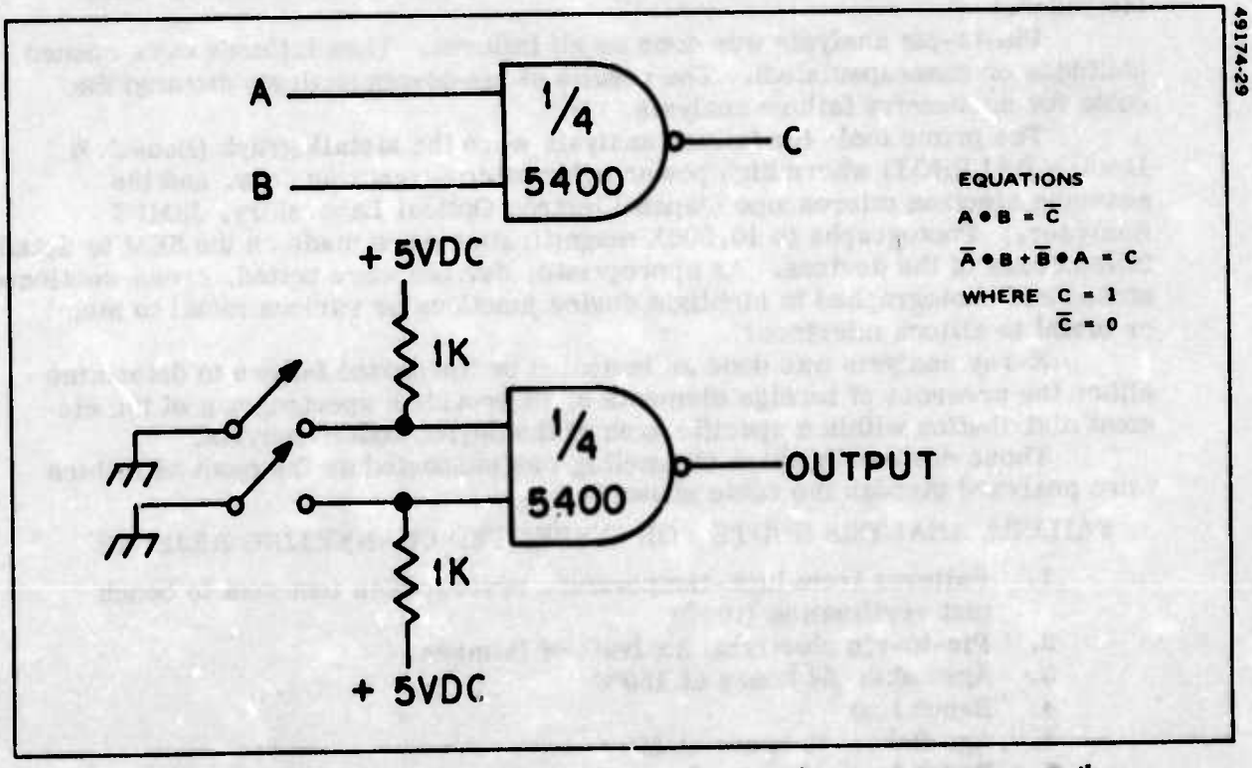


Figure 53. Bench Test Circuit and Conditions for Comfirming Logic Gate Failures

4. FAILURE ANALYSIS METHODS

High magnification color photographs, X-ray analysis, and scanning electron microscope (SEM) pictures were taken or failed devices after stress testing to pinpoint failed areas for defective elements.

Prior to module fabrication, all devices were 100% visually inspected. Visual anomalies were noted as potential future failures but no devices were rejected at this point. After module fabrication, each module was visually inspected and electrically tested. At this point, any assembly rejects were removed from the test. The good devices were forwarded to the screen and stress test sequences, and the bad devices were routed to failure analysis. As reject devices were received they were analyzed according to the route shown in Figure 54. Only devices classified as catastrophic failures were eliminated at each screen/stress test interval. Because of the high number of failures at first electrical test it was decided to liberalize the device acceptance criteria to ensure that some devices would survive all seven screen/stress tests. Thus, functioning devices, even though out of spec, were continued through the tests until they became catastrophic failures.

All failures were verified on a bench test set-up. (Details of the electrical failure verification are given in the preceding topic, "Electrical Test Methods".)

Pin-to-pin analysis was done on all failures. Then failures were opened (delidded or unencapsulated). The results of pin-to-pin analysis dictated the route for successive failure analysis.

The prime tools for failure analysis were the Metallograph (Bausch & Lomb – BALPHOT) where high power color microscopy was done, and the scanning electron microscope (Japan Electron Optical Laboratory, JSMU3 Analyzer.) Photographs to 10,000X magnification were made on the SEM to detail failed areas of the devices. As appropriate, devices were potted, cross-sectioned, etched and photographed to highlight device junctions or various metal to metal or metal to silicon interfaces.

X-ray analysis was done as indicated by the device failure to determine either the presence of foreign elements or to provide a spectrogram of the element distribution within a specific area of the device under analysis.

Those devices in which channeling was suspected as the mode of failure were analyzed through the route shown below.

FAILURE ANALYSIS ROUTE FOR SUSPECTED CHANNELING REJECTS

1. Failures from high-temperature reverse bias test sent to bench test verification (100%)
2. Pin-to-pin electrical analysis of failures
3. Age bake: 24 hours at 150°C
4. Bench test
5. Age Bake: 30 hours at 150°C
6. Bench test
7. High-temperature reverse bias test: 168 hours
8. Bench test
9. Data Accumulation
10. Data Analysis

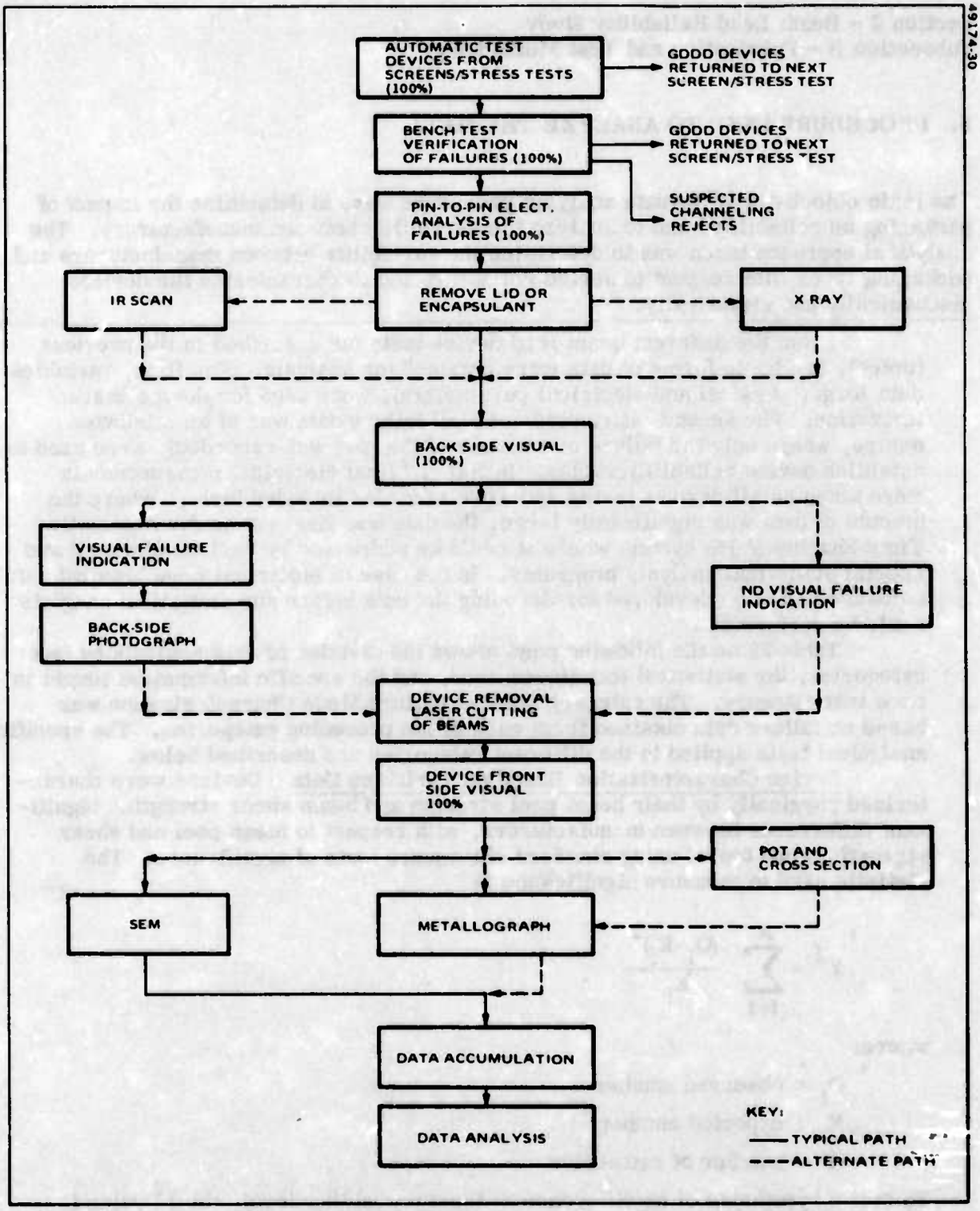


Figure 54. Primary Device Failure Analysis Route. The primary tools for failure analysis were the metallograph and the scanning electron microscope.

5. PROCEDURE USED TO ANALYZE THE DATA

The main objectives of the data analysis procedure were to determine the impact of packaging on reliability, and to analyze the variability between manufacturers. The analytical approach taken was to determine the variability between manufacturers and packaging types with respect to device reliability and to characterize the devices mechanically and electrically.

From the different beam lead device tests (as described in the previous topics), two basic forms of data were obtained for analysis. The first, variables data (e.g., physical and electrical parameters), were used for device characterization. The second, attributes data (all failure data was of an attributes nature, where only the failure or success of the part was recorded), were used to establish device reliability values. Initial and final electrical measurements were taken on all devices tested and were recorded in coded form. Where the amount of data was significantly large, the data was first put on the Automatic Time Sharing (ATS) system where it could be addressed by various standard and special statistical analysis programs. In the case of electrical measurement data software had to be developed for decoding the data before any statistical analysis could be performed.

Table 22 on the following page shows the division of data analysis by test categories, the statistical techniques used, and the specific information sought in each test category. The category labeled Failure Mode Characterization was based on failure data obtained from each of the preceding categories. The specific analytical tests applied to the different categories are described below.

Device Characterization Based on Variables Data – Devices were characterized physically by their beam peel strength and beam sheer strength. Significant differences between manufacturers, with respect to mean peel and shear strength, were tested using standard chi-square tests of significance. The statistic used to measure significance is

$$\chi^2 = \sum_{i=1}^{N} \frac{(O_i - E_i)^2}{E_i}$$

where:

O_i = observed number

E_i = expected number

N = number of categories

To test a hypothesis of no difference at the α probability level, the χ^2 value is compared to a standard chi-square table using N-1 degrees of freedom (df).

In order to characterize device behavior during stress testing, the means and standard deviations of all electrical parameters were estimated from measurements on device samples, both initially and after all testing had been conducted.

The mean parameter drift and standard deviation for each device type was then estimated and tested for significance using the t-test. The statistic used for the t-test is:

$$t = \frac{\bar{x}_1 - \bar{x}_2}{S\sqrt{\frac{1}{n_1} + \frac{1}{n_2}}}$$

where:

$\bar{x}_1$, $\bar{x}_2$ are the sample means of the two populations

n_1, n_2 are the respective sample sizes

$$S = \sqrt{\frac{n_1 S_1^2 + n_2 S_2^2}{n_1 + n_2 - 2}}$$ (the pooled variance)

S_1, S_2 are the sample variances.

To test the hypothesis of no difference at the α probability level, the t value is compared to a standard t-table using $n_1 + n_2 - 2$ degrees of freedom.

Techniques for Analyzing Attributes Data – Factorial designs were used to analyze the effects of packaging on device reliability. Since the failure data consisted of counts of successes and failures, the sample proportion, p, was used as a relative measure of device reliability. In order to use analysis of variance (ANOVA) techniques for analyzing packaging effects on reliability, the sample proportions were normalized using the arcsin transformation:

$$Z = \arcsin \sqrt{P} \ ,$$

where P is in percentage of failed devices under some factorial design. Z is normally distributed with variance equal to 821/n degrees, where n is the common sample size. In cases where cell sizes are significantly unequal, a weighted ANOVA is required. The method used in this case is the "method" of weighted squares of means" (Reference: Principles and Procedures of Statistics by Steel & Torrie, Chapter 13).

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TABLE 22. STATISTICAL TECHNIQUES AND ANALYTICAL OBJECTIVES FOR EACH TEST CATEGORY

Test Category	Statistical Techniques	Analysis Objectives
Device Characterization: physical and electrical tests on devices as supplied by vendors	Analysis of Variance Mean, standard deviation, goodness-of-fit tests	Variability of manufacturers Distribution of performance parameters
Packaging Impact on Reliability	Statistical hypothesis test Analysis of Variance	Necessity of hermetic seal Differences in plastic coating methods.
Screening and QC Procedures	Analysis of Variance	Effect of stress and stress-sequence on the frequency of failure
Device Characterization: after screening and stress tests (final electrical tests)	Mean, standard deviation Tests of significance (t-tests)	Variability of manufacturer Variability due to complexity Distribution of performance parameters
Failure Mode Characterization	Variance analysis using contingency analysis	Variability of manufacturers Variability due to complexity

1. RESULTS OF THE SCREENING AND STRESS TESTS

The number of devices that failed the screening and stress tests are collected and identified here. The data is tabulated according to test type, packaging, vendor, class, complexity, and combinations of these categories.

After the beam lead devices were fabricated in both hermetic packages they were 100% electrically tested and then put through the screens and stress tests detailed in a previous subsection. The device yields through the stress tests, categorized by variations such as device manufacturer, complexity, class, and package are shown in Tables 23 through 29. In Table 23 it is seen that 2112 devices are shown as going into first electrical test. This is in apparent contrast to the 3,456 devices called for in the full factorial experimental design. The difference is explained as follows.

After first electrical test it became obvious that unprotected beam lead devices would not survive in adverse environments. At the conclusion of the first electrical test, over 90% of the 972 devices (486 sealed with deionized water and 486 devices sealed with saline solution) failed catastrophically. (Eventually all of the H_2O and saline solution devices failed.) Therefore, the data from these devices was not presented in the tables. In addition to the 972 devices not shown, 216 devices (12 cells) were not included because of late vendor delivery. Another 156 devices were dropped because they were actual or probable assembly or test caused rejects. Thus, only 2112 devices are shown in the tables.

The statistical significance of the data presented in the tables will be discussed in a later subsection.

TABLE 23. BEAM LEAD SCREENING AND STRESS TEST FAILURES

Screen/Stress Test	Devices into Test	Devices Failed Test	% Failed
First Electrical	2112	198	9.3
High temperature storage	1914	30	1.5
Temperature cycle	1884	18	0.9
Thermal shock	1866	8	0.4
168 Hrs HTRB	1858	178	9.5
1000 Hrs HTRB	1680	122	7.2
168 Hrs bias moisture life	1558	147	9.4
1000 Hrs bias moisture life	1411	296	21.0
Boiling H_2O	1115	199	17.8
Salt atmosphere	916	133	14.5
Totals	2112	1329	62.9

TABLE 24. BEAM LEAD SCREENING AND STRESS TEST FAILURES BY SCREEN AND DEVICE CLASS

	Digital			Linear		
	Tested	Failed	% Failed	Tested	Failed	% Failed
First Electrical Test	979	74	7.6	1133	124	10.9
High Temperature Storage	905	10	1.1	1009	20	2.0
Temperature Cycle	895	12	1.3	989	6	0.6
Thermal Shock	883	5	0.6	983	3	0.3
168 Hours HTRB	878	14	1.6	980	164	16.7
1000 Hours HTRB	864	13	1.5	816	109	13.4
168 Hours Bias Moisture Life	851	15	1.8	707	132	18.7
1000 Hours Bias Moisture Life	836	131	15.7	575	165	28.7
Boiling H_2O	705	103	14.6	410	96	23.4
Salt Atmosphere	602	70	11.6	314	63	20.1
Totals		447	45.6		882	77.8

TABLE 25. BEAM LEAD SCREENING AND STRESS TEST FAILURES BY VENDOR

Vendor	Devices into Test	Devices Failed Test	Percent Failed
W	934	544	58.2
X	420	212	50.5
Y	260	242	93.0
Z	498	331	66.5

TABLE 26. BEAM LEAD SCREENING AND STRESS TEST FAILURES BY VENDOR AND DEVICE CLASS

	Vendor	Devices into Test	Devices Failed Test	Percent Failed
Linear Devices	W	479	381	79.5
	X	153	78	50.9
	Y	260	242	93.0
	Z	241	181	75.1
Digital Devices	W	455	163	35.6
	X	267	134	50.2
	Y	–	–	–
	Z	257	150	58.4

TABLE 27. BEAM LEAD SCREENING AND STRESS TEST FAILURES BY CLASS AND COMPLEXITY

		Devices into Test	Devices Failed Test	Percent Failed
Linear	Simple	909	691	76.0
	Complex	224	191	85.3
Digital	Simple	524	238	45.4
	Complex	455	209	45.9

TABLE 28. BEAM LEAD SCREENING AND STRESS TEST FAILURES BY PACKAGE TYPE AND DEVICE CLASS

		Devices into Test	Devices Failed Test	Percent Failed
Linear	Hermetic	206	179	86.9
	Non-hermetic	927	703	75.8
Digital	Hermetic	201	55	27.4
	Non-hermetic	778	392	50.4

TABLE 29. BEAM LEAD SCREENING AND STRESS TEST (HTRB) FAILURES BY VENDOR AND CLASS

	Digital			Linear		
Vendor	Tested	Failed	% Failed	Tested	Failed	% Failed
After 168 hours HTRB (0 – 168 hours)						
W	396	7	1.8	390	53	13.6
X	254	0	0.0	145	6	4.1
Y	–	–	–	242	75	31.0
Z	228	7	3.1	203	30	14.8
After 1000 hours HTRB (168 hours to 1000 hours)						
W	389	8	2.1	337	62	18.4
X	254	1	0.4	139	0	0.0
Y	–	–	–	167	32	19.2
X	221	4	1.8	173	15	8.7

Note: Vendors X and Y used <100> silicon orientation
Vendors W and Z used <111> silicon orientation

2. RESULTS OF FAILURE ANALYSIS: CATEGORIZING THE FAILURES

A sampling of 273 of the failed devices were selected to be failure analyzed in detail to determine the cause of failure and the distribution of failures within the variables studied. As expected, linear devices exhibited a higher incidence of failures.

The failed devices were selected according to an unbalanced factorial design. (A balanced factorial sample was attempted but not possible to accomplish due to the limited number of failures from some tests and treatments.) Here samples were gathered from each screen/stress and test sequence, package treatment, vendor, and device type. This provided a statistically representative sampling of all of the variables and combination of variables under study.

After each screen and stress test, the device failures were retested on the bench to verify the failure, electrically analyzed pin-to-pin, and 100 percent visually analyzed. The criteria for determining a "failed" device was the electrical performance. The device failure mode was then categorized according to cause: general semi-conductor failures (standard processing related defects), environmentally induced failures, beam-lead-processing related failures, or other failure mechanisms such as channeling or those peculiar to a vendors processing technique. Table 30 summarizes the failures according to device type. Considerable data was obtained on environmentally induced failures and failures directly (or indirectly) related to the beam lead processing; this data is given in the following topics.

Electrical Failure Indications – In general, the failures were catastrophic. Devices with degraded parameters but which were operational were continued to the next screen or stress test. The general electrical failure indications for all rejects were:

- Digital Devices – (SC 148, 149, 150, 151)
  Latch up in one or more logic states due to gating circuit transistor failure caused by multi-emitter transistor or output transistor open or short.
- Linear Devices – (SC 152, 153, 154, 155, 156)
  Devices sitting at (+) or (-) power supply voltage due to output stage transistors being shorted, input transistors being defective, or surface inversion.

General Semi-conductor Design or Processing Failures – The majority of the failures shown in Table 30, 163/273 or 59.7%, were caused by internal opens or shorts within the device. Detailed failure analysis could not pin-point any definite cause of failure. It is thus assumed that these failures are not specifically beam lead device oriented but are general semi-conductor failures. In the case of the SC 148, the thermal maps done during device characterization showed up a hot spot in the device which roughly correlates to a high incidence of blown diodes in that area on the beam lead device. Photographs of some of the types of failures defined as opens and shorts are shown in Figures 55 and 56.

Anticipated Failure Modes – Failure modes which were looked for, but not found, were sodium ion penetration and platinum migration. Several of the devices that were sealed with saline solution were decaped, screened and microprobed on the SEM. No evidence of sodium ions was found beneath the silicon nitride.

Several internally shorted devices, particularly those which had seen high temperatures for the longest time (devices failing after HTRB or Biased Moisture Life) were potted, cross-sectioned, and microprobed on the SEM. No evidence of platinum migration was found.

Other Anomalies – Other device failures that were not part of the sample shown in Table 30, but are noteworthy, are shown in Figures 57 and 58. Figure 57 shows missing sections of gold interconnect metal. This indicates either a mask breakdown or contamination during the deposition of gold over the platinum. Figure 58 shows a defect peculiar to vendor Y's beam lead processing. Vendor Y does no gold sputtering over the platinum but plates directly over the platinum to build up the interconnect metal. This results in gold roll back from the edges of the platinum along with hot spots along the conductors.

TABLE 30. DEVICE FAILURE MODE ANALYSIS

	DIGITAL DEVICES				LINEAR DEVICES					
CODE VENDOR TYPE / CAUSE OF FAILURE	SC148 W 5473	SC149 X RF100	SC150 W 5400	SC151 Z 5410	SC152 W 741	SC153 Y 741	SC154 Z 741	SC155 X RM101	SC156 W 710	TOTAL DEVICES ANALYZED
Gold Migration	1	5	2	4	6	4	8	5	10	45
Interconnect Shorts	1			1	2	2			1	7
Interconnect Delamination					1				1	2
Exposed Junctions		1			4					5
Channeling	1	1		2	5	7	10	6	6	38
Nitride Voids	1	2	1	1	2	2	1	1	2	13
Shorted Devices (Internal)	9	15	11	9	15	13	11	6	14	103
Open Device (Internal)	5	5	8	11	7	6	8	4	6	60
TOTAL	18	29	22	28	42	34	38	22	40	273

NOTE: Moisture and Saline Solution rejects are not included in these totals.

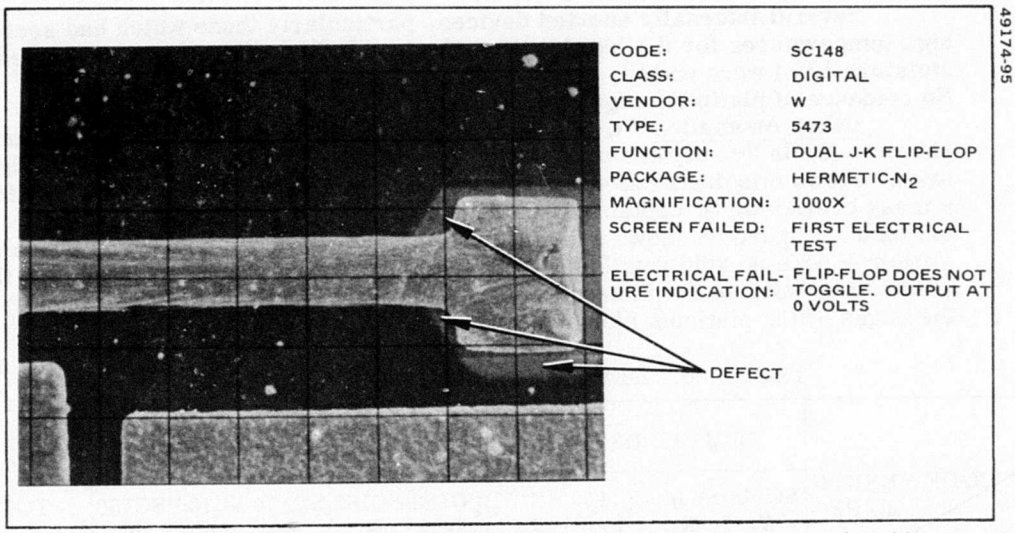


Figure 55. SC148 with Blown Diode Showing Surface Diffusion of Gold

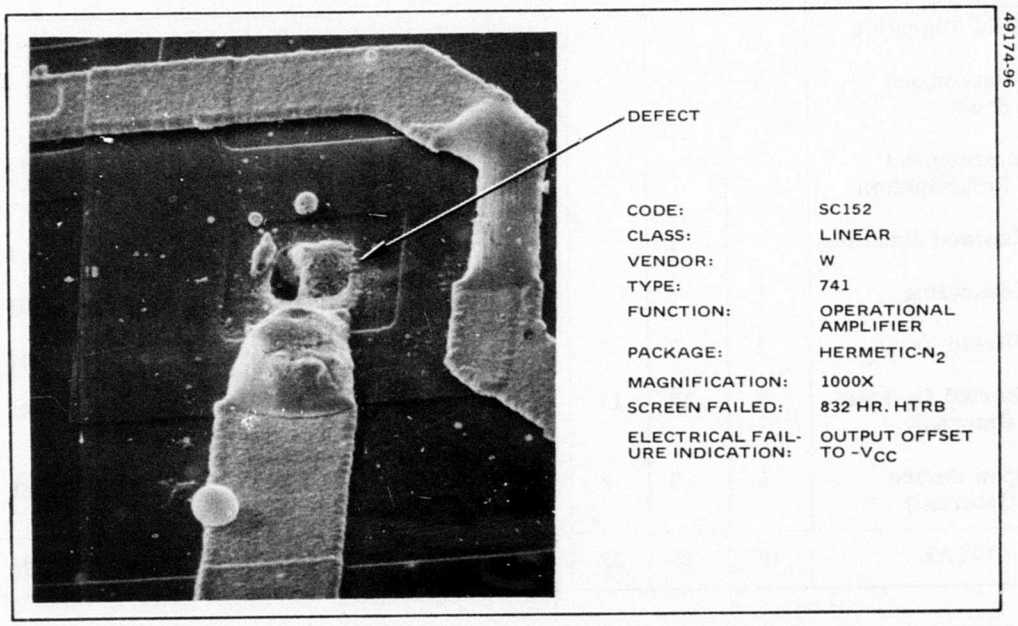


Figure 56. SC152 with Shorts, Melted Gold, Blown Junctions

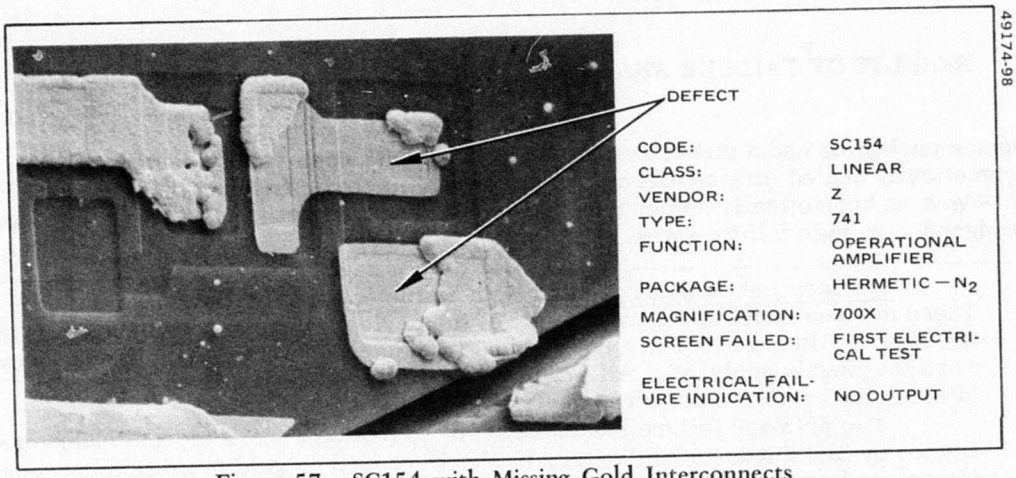


Figure 57. SC154 with Missing Gold Interconnects

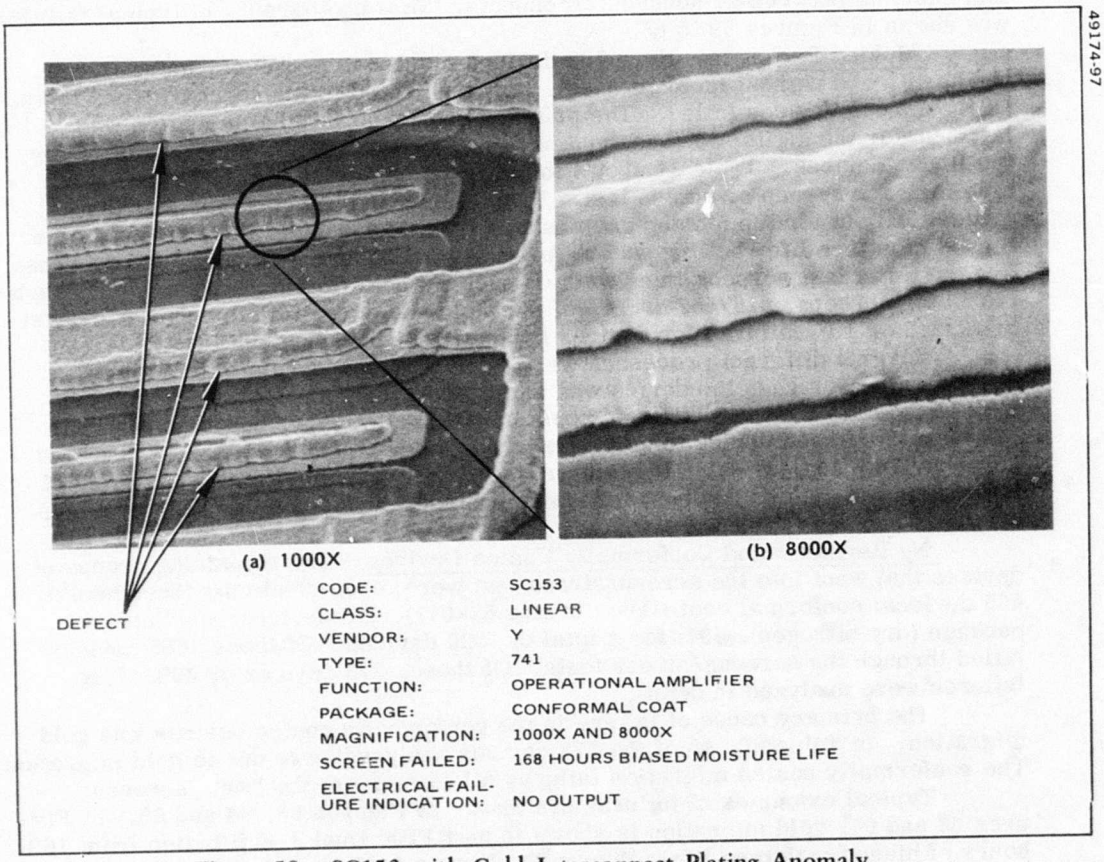


Figure 58. SC153 with Gold Interconnect Plating Anomaly

3. RESULTS OF FAILURE ANALYSIS: ENVIRONMENT INDUCED REJECTS

Device packaging had a direct bearing on failures with conformally coated and hermetically sealed (dry nitrogen) devices producing fewer failures than molded packages or hermetically sealed packages containing moisture. The "wet" screens produced very high failure rates.

Devices Hermetically Sealed With Saline Solution or Deionized Water – These devices represent a majo. part of the device failures encountered during the study. Although they are not carried in the screen/stress data tables, they were thoroughly analyzed. All 972 devices from these two groups eventually failed. Most failures occurred at first electrical test.

The primary failure modes were; a) shorts between adjacent conductors caused by moisture and salt water, b) shorts caused by gold migration between adjacent conductors, c) corrosion of gold-interconnections with metal breaking free and shorting between adjacent interconnects. SEM photographs of typical failures are shown in Figures 59 to 65.

Molded Packages – Here 792 devices molded in packages, using Hysol C-59 (with and without mold release), were subjected to the screen/stress tests. Of these, 641 devices failed. The primary electrical failure indication was latch-up for the digital devices, and devices setting at power supply voltage for the linear devices. Table 31 shows the failures by device class and package type for each screen or stress test. From Table 31 it can be seen that the largest fall out for the molded devices was from high temperature reverse bias, biased moisture life, boiling water, and salt atmosphere. Of particular interest are the three last screens (the "wet" or package qualification screens). Through the "wet" screens, 416/567 or 74% of the molded devices failed. This compares to 40/213 or 19% failures for devices hermetically packaged with N_2.

Several different processes were tried to de-encapsulate the molded devices. In each case the device was damaged to the point that no meaningful visual or detailed failure analysis could be done. However, based on the ratio of molded packaged device to hermetic package device failures through the "wet" screens, 74%/19% (or 4:1), it seems reasonable to assume that the majority of failures in the molded devices were "environment" induced as a result of a non-hermetic package.

N_2 Hermetic and Conformally Coated Devices – The remaining groups of devices that went into the screen/stress test were: conformal coat (Scotchcast), 465 devices; conformal coat (Dow Corning 62-047), 448 devices; and hermetic package (dry nitrogen), 407; for a total of 1320 devices. Of those, 688 devices failed through the screens/stress tests. Of these, 273 devices or 40% of the failures were analyzed in detail.

The primary cause of failure in the conformally coated devices was gold migration. In Table 30, 45 of the 273 devices analyzed were due to gold migration. The conformaily coated migration failures all came from the "wet" screens.

Typical examples of failures are shown in Figures 63, 64 and 65. In Figures 63 and 64, gold migration is shown in an RF100 Dual J-K flip-flop from 168 hours of biased moisture life. Figure 65 shows a 5473 Dual J-K flip-flop which failed somewhere between 168 and 1000 hours of biased moisture life. In Figure 65, part of the conformal coating was left intact for comparison.

TABLE 31. DEVICE FAILURES AS A FUNCTION OF DEVICE CLASS & PACKAGE TYPE

Package Type	Devices Tested and Failed*			First Electrical		High Temp. Storage		Temperature Cycle		Thermal Shock		1000 hours HTRB		1000 hours Bias Moisture Life		Boiling Water		Salt Atmosphere	
	Total	Digital	Linear	D	L	D	L	D	L	D	L	D	L	D	L	D	L	D	L
Conformal Coat Scotch Cast	250 (465)	62 (211)	188 (254)	12	20	7	2	0	1	2	0	3	40	9	79	14	25	15	21
Conformal Coat-Dow Corning	204 (448)	61 (204)	143 (244)	6	14	0	1	0	1	1	1	3	21	20	48	19	34	12	23
Molded Release	322 (405)	150 (203)	172 (203)	35	24	0	0	1	1	1	2	6	54	54	67	32	15	21	9
Molded No Release	319 (387)	119 (160)	200 (227)	13	32	0	5	1	1	1	0	5	43	58	88	29	22	12	9
Dry Nitrogen	234 (407)	55 (210)	179 (206)	8	34	3	12	10	2	0	0	10	115	5	15	9	0	10	1
Totals	1329 (2112)	447 (979)	882 (1133)	74	124	10	20	12	6	5	3	27	273	146	297	103	96	70	63

*Numbers in parentheses are total devices submitted at beginning of testing.

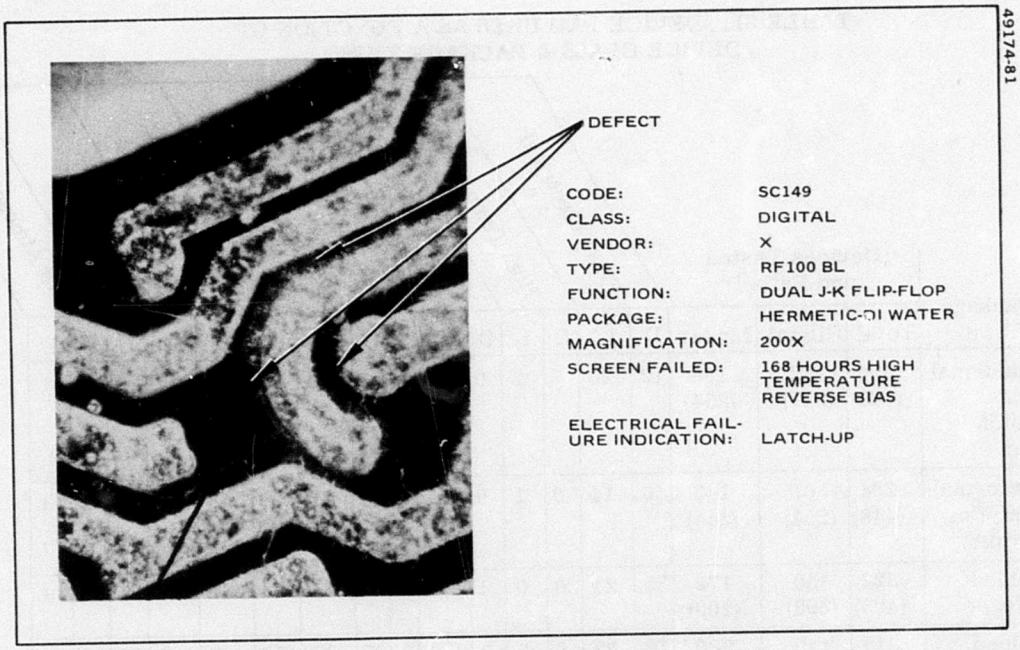


Figure 59. SC149 with Gold Migration

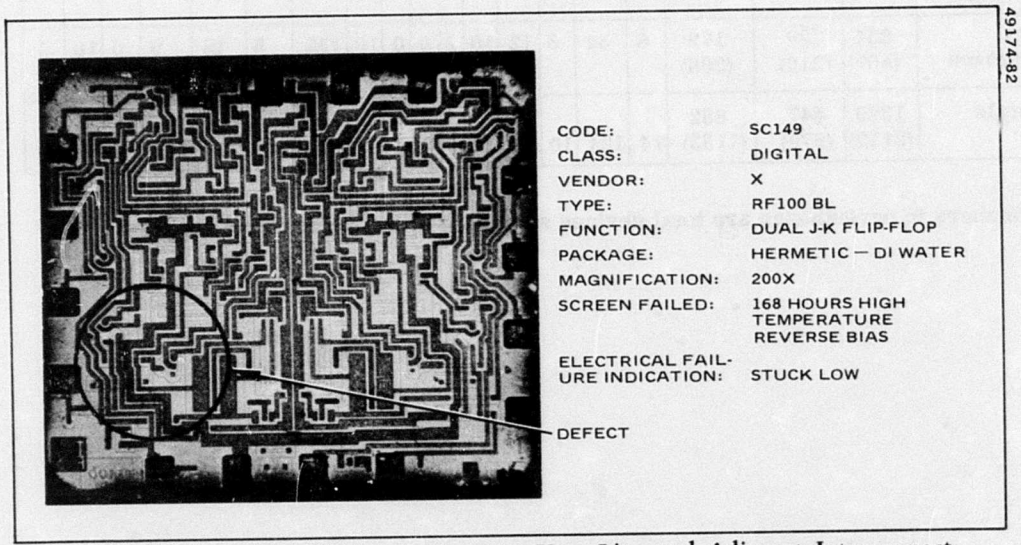


Figure 60. SC149 with Arcing Between V_{CC} Line and Adjacent Interconnect

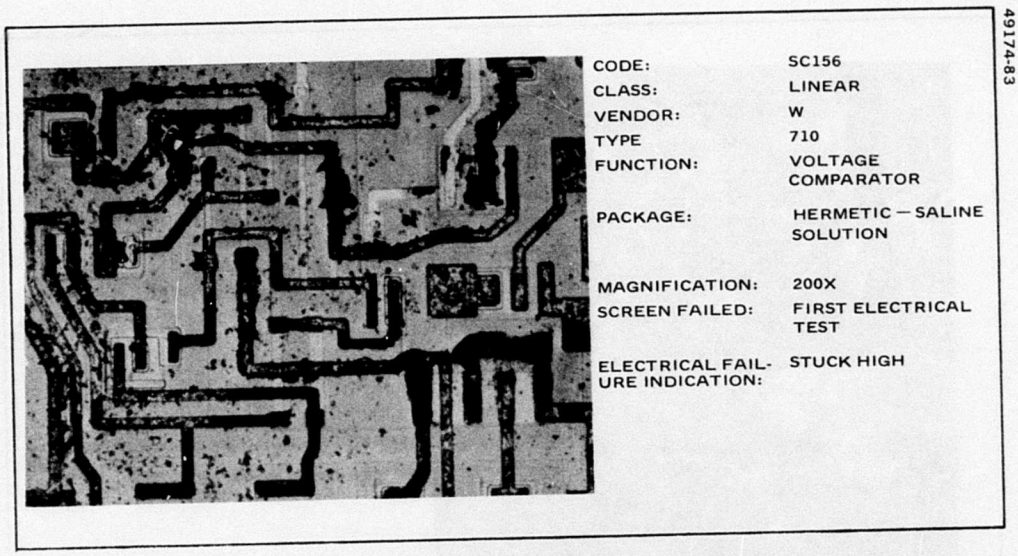


Figure 61. SC156 with Corrosion (Across Entire Surface)

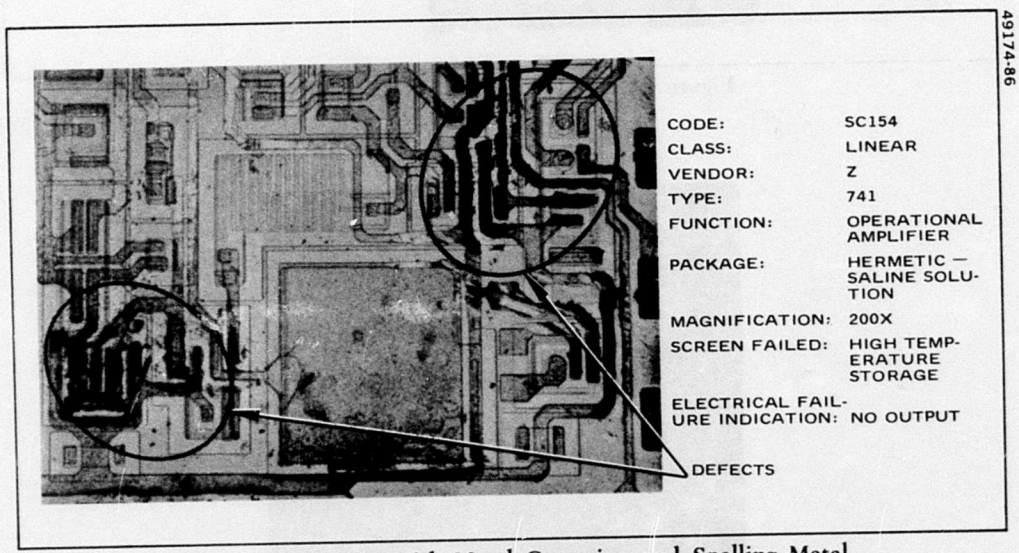


Figure 62. SC154 with Metal Corrosion and Spalling Metal

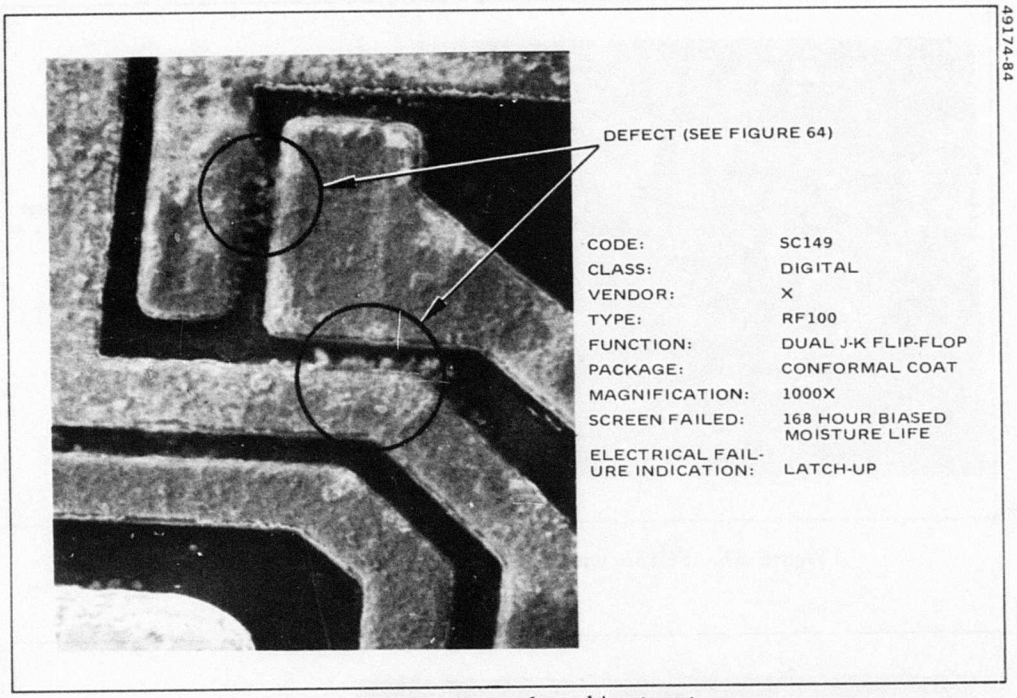


Figure 63. SC149 with Gold Migration

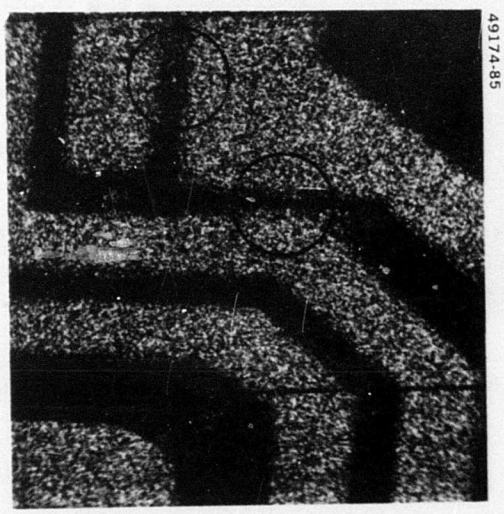


Figure 64. 1000X SEM X-Ray Scan of Figure 63 Definitely Confirming Gold as the Migrating Metal

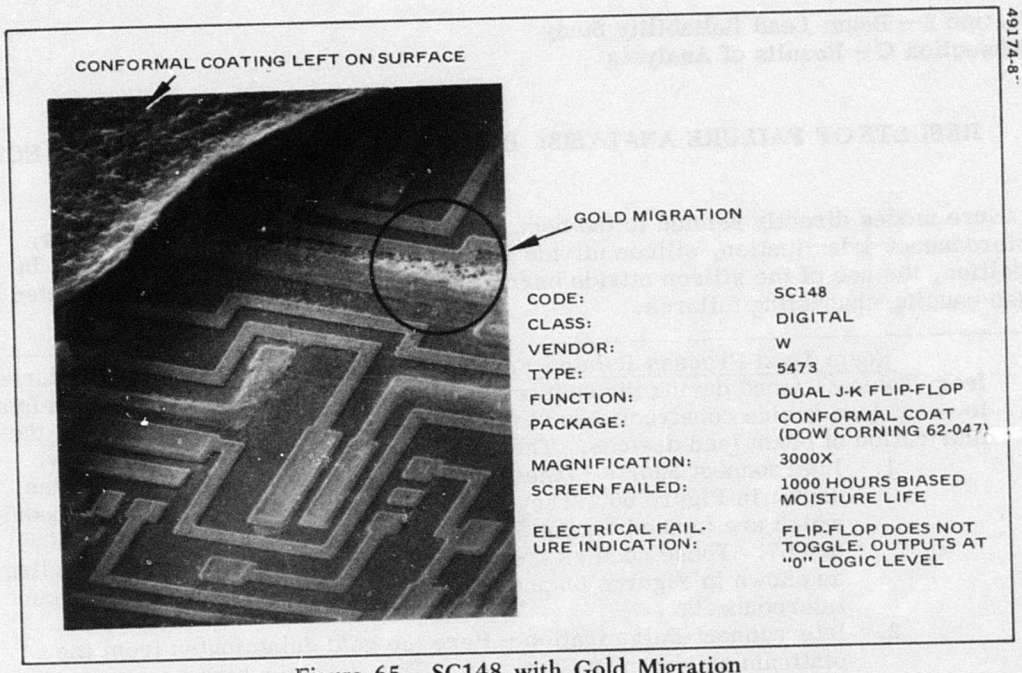


Figure 65. SC148 with Gold Migration

4. RESULTS OF FAILURE ANALYSIS: BEAM LEAD PROCESS INDUCED REJECTS

Failure modes directly related to the beam lead process are interconnect shorts, interconnect delamination, silicon nitride voids, and exposed device junctions. In addition, the use of the silicon nitride barrier in the beam lead device is suspected of also causing channeling failures.

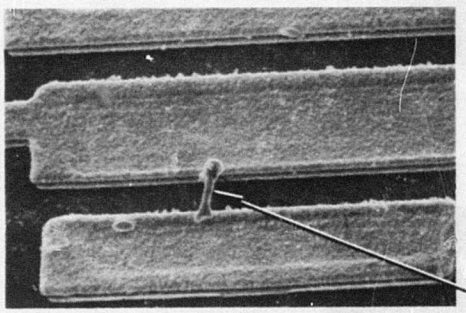
Beam Lead Process Related Failures – Several modes of device failures from Table 31 found during the course of failure analysis are specifically related to beam lead device construction or to the processing steps involved during the fabrication of beam lead devices. These failure modes are described below.

1. Interconnect Shorts – These can be caused by "plating" bridges as shown in Figure 66. They can also be caused by spalling gold nodules which are formed during the gold plating process as shown in Figure 67. These nodules then break loose during temperature cycling as shown in Figures 68 and 69 causing a short between two adjacent interconnects.
2. Interconnect Delamination – Here the gold delaminates from the platinum as shown in Figure 70. This causes a high resistance in a length of the conductor eventually causing the device to open.
3. Voids in Nitride – In this case, the hole in the nitride allows for intrusion of moisture or other contaminants causing the device to fail. This is shown in Figure 71.
4. Exposed Junctions – This failure mode is primarily caused by mask misalignment during the photolithography process. A typical case is shown in Figure 72.

Channeling Failures – Prior to the wide spread use of channel stops or guard rings it was common to subject pnp transistors to 168 hours of high temperature reverse bias to weed out the channeling rejects. From the number of beam lead device failures through the HTRB screens, it seems that these devices, by virtue of both their complexity and the number of dielectric layers in their construction, are prone to channeling. From Table 24, it can be seen that 1858 devices went into the high temperature reverse bias (HTRB) screen and that 178 failed after 168 hours, and after 1000 hours an additional 122 devices failed. This represents a failure of 300/1858 or 16.1%. Even more significant is the ratio of linear to digital device failures, through 168 hours of HTRB. Here, 14/878, or 1.6% of the digitals failed while 164/980 or 16.7% of the linears failed. Through 1000 hours of HTRB, overall the failures were 27/878 or 3.1% for the digital devices and 273/980 or 27.9% for the linear devices. Thus the ratio of linear to digital failures through HTRB was thus about 10:1.

Table 29 shows HTRB device failures as a function of vendor, class and silicon orientation. Although it has been reported that <100> oriented devices are more susceptible to channeling than <111> oriented devices, the data in Table 29 does not apparently show this relationship. Also of interest is that channel stops were used by vendor Y, while vendors W & Z did not use channel stops. The use of channel stops by vendor X was indeterminate.

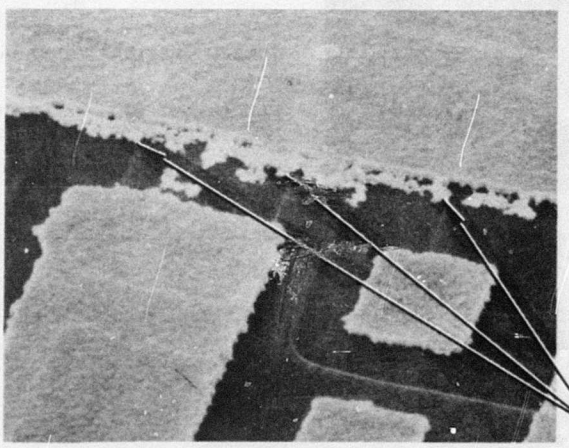
All HTRB failures, particularly the linear devices, were channeling suspects. These failures followed the route for Failure Analysis detailed in a previous subsection. Here, the failures were confirmed at bench test and then they were age baked at 150°C for 24 hours. Approximately 25% of the devices recovered after 24 hours. The remaining failures were then placed in an oven for an additional 30 hours. Here about 20% of the devices again recovered. The "recovered" devices were then returned to HTRB for 168 hours. They were retested after HTRB and all failed. Of the devices randomly sampled for failure analysis and shown in Table 30, 38 device failures were classified as caused by channeling. Of these, channeling failures represent 38/273 or 14% of the devices analyzed. Of these, 4/273 or 1.5% were digital while 34/273 or 12.5% were linear. This correlates with the higher degree of susceptibility of channeling inherent in the linear devices.



CODE:	SC148
CLASS:	DIGITAL
VENDOR:	W
TYPE:	5473
FUNCTION:	DUAL J-K FLIP-FLOP
PACKAGE:	HERMETIC N_2
MAGNIFICATION:	1000X
SCREEN FAILED:	FIRST ELECTRICAL TEST
ELECTRICAL FAILURE INDICATION:	OUTPUTS HIGH

49174-88

Figure 66. SC148 with an External Short



CODE:	SC151
CLASS:	DIGITAL
VENDOR:	Z
TYPE:	5410
FUNCTION:	TRIPLE 3 INPUT NAND GATE
PACKAGE:	BARE CHIP
MAGNIFICATION:	1000X
SCREEN FAILED:	FIRST VISUAL INSPECTION
ELECTRICAL FAILURE INDICATION:	THIS TYPE OF DEFECT LED TO THE REJECTS SHOWN IN FIGURE 68 AND 69

49174-89

Figure 67. SC151 with Poor Metal Definition

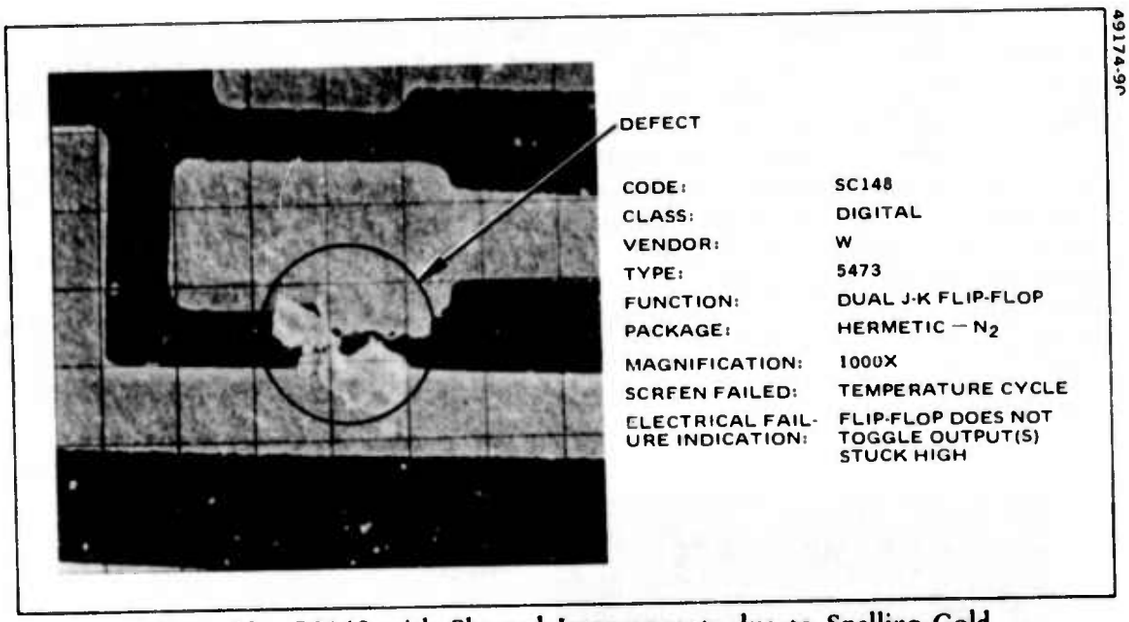


Figure 68. SC148 with Shorted Interconnects due to Spalling Gold

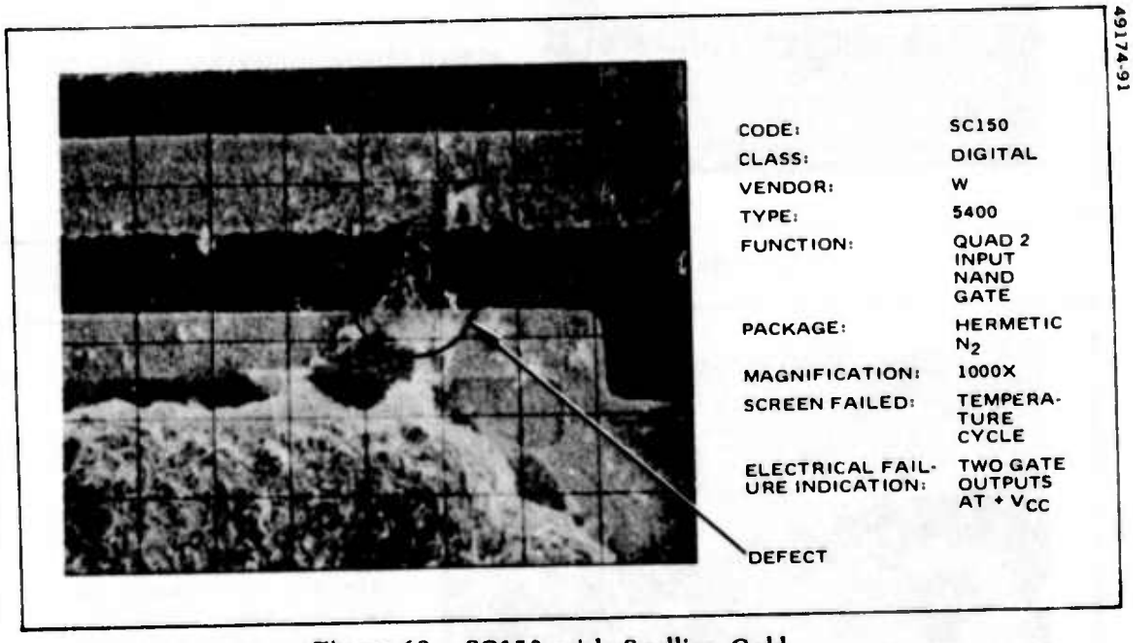
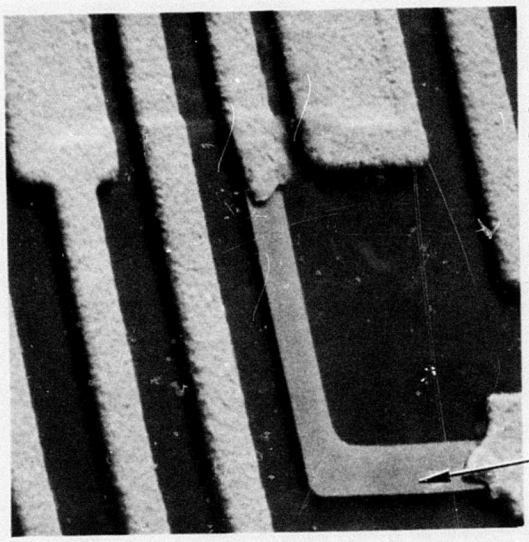


Figure 69. SC150 with Spalling Gold

Here the spalling gold has shorted two adjacent interconnects. This created a hot spot resulting in the gold-silicon puddled area shown

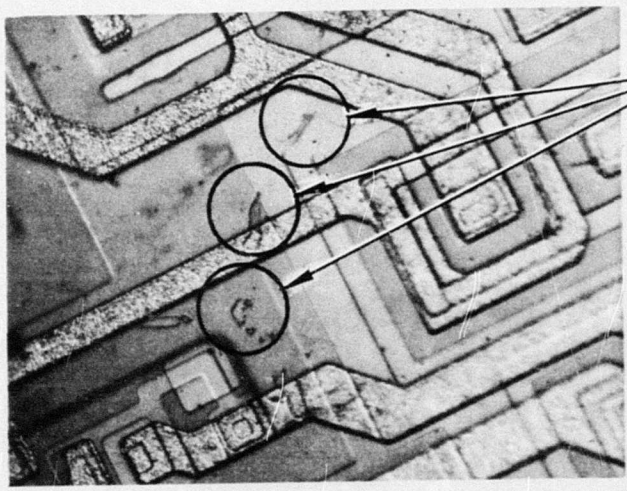


49174-92

CODE:	SC148
CLASS:	DIGITAL
VENDOR:	W
TYPE:	5473
FUNCTION:	DUAL J-K FLIP-FLOP
PACKAGE:	HERMETIC, N_2
MAGNIFICATION:	1000X
SCREEN FAILED:	THERMAL SHOCK
ELECTRICAL FAILURE INDICATION:	FLIP-FLOP DOES NOT TOGGLE OUTPUTS STUCK IN "0" LOGIC LEVEL

DEFECT

Figure 70. SC148 with Gold Delamination Resulting from Thermal Shock



49174-93

DEFECT

CODE:	SC154
CLASS:	LINEAR
VENDOR:	Z
TYPE:	741
FUNCTION:	OPERATION AMPLIFIER
PACKAGE:	CONFORMAL COAT
MAGNIFICATION:	200X
SCREEN FAILED:	168 HOURS BIASED MOISTURE LIFE
ELECTRICAL FAILURE INDICATION:	OUTPUT OFFSET TO $+V_{CC}$

Figure 71. SC154 with Voids in Nitride

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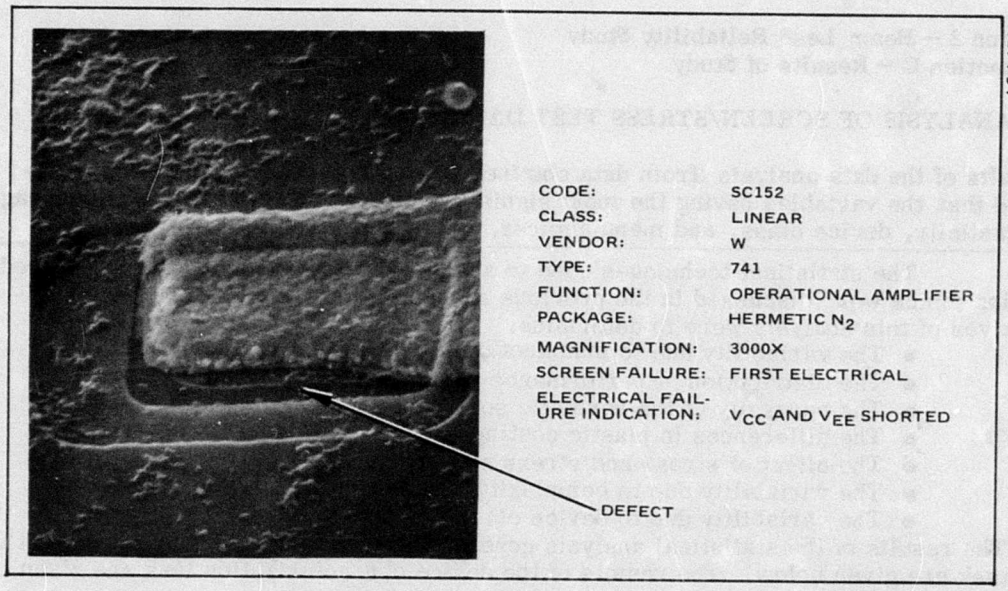

Figure 72. SC152 with Exposed Junction. Although this particular unit was from the N_2 hermetically sealed group, the majority of the exposed junction failures were from the conformally coated and molded package groups. Here, as moisture and other contaminants invade the junction areas, the junction becomes electrically leaky or fails due to metal migration through discontinuities in the platinum. Metal migration in beam lead devices through this mode has been reported by other researchers.

5. ANALYSIS OF SCREEN/STRESS TEST DATA

Results of the data analysis (from data obtained from the screen/stress tests) indicated that the variables having the most significant impact on reliability were package hermeticity, device class, and manufacturer.

The statistical techniques used to analyze the data described in the preceding topics were discussed in the previous subsection (see Table 22). The objectives of this analysis were to determine:

- The variability due to manufacturers
- The distribution of performance parameters
- The necessity of the hermetic seal
- The differences in plastic coatings
- The effect of stress and stress sequence
- The variability due to complexity
- The variability due to device class

The results of the statistical analysis generated from the screen and stress test task are given below. The results of the device characterization task are given in the next topic.

Device Failure Mode Characterization – The dependence of device failure mode upon device manufacturer, class, complexity and package hemeticity is given in Table 32. Some key failure mode relationships of note are:

1. Gold migration is dependent only on package hermeticity.
2. Channeling is independent of device manufacturer but highly dependent upon device class.
3. Internally shorted devices are highly dependent upon device complexity.
4. Beam metallurgy processing failures are manufacturer dependent.
5. Failures due to Nitride voids and to exposed junctions are dependent upon package hermeticity.
6. Internal device opens were independent of all variables studied.

Package Hermeticity – The package hermeticity was of significant importance. However, at first glance the data seems to indicate little difference between the failure rate of hermetically sealed devices (57.5%) and non-hermetically sealed devices (64.2%). But when the failure rates are examined according to device class (see Table 28), and taking into account the higher incidence of failures in linear devices (greater than 75 percent for both hermetically and non-hermetically sealed), the failure incidence of (digital) hermetically sealed devices (sealed in a TO-8 can with dry nitrogen) was significantly less than conformally coated or molded packages: 27.4% compared to 50.4%.

Although no gold migration failures were found in the N_2 hermetically sealed devices, it is recognized (as reported in other research sponsored by RADC) that even hermetically sealed devices with acceptable leak rates can contain moisture levels in the range of 1% that can cause device failures.

Plastic Package – The conformally coated devices had a lower failure incidence than molded packages.

Sequence of Screening and Stress Tests – There was no significant difference in device failure incidence among the three screening sequences used.

Device Manufacturer – The rank, according to incidence of failures is:

Vendor	Rank
X	1
W	1
Z	2
Y	3

Where 3 is least accpetable.

Device Complexity – Device complexity was not a significant factor in device failure incidence.

Device Class – The incidence of failures in linear devices was significantly higher than in digital devices.

TABLE 32. DEVICE FAILURE MODE DEPENDENCY

Dependent Upon \ Failure Mode	Gold Migration	Interconnect Shorts	Interconnect Delamination	Exposed Junctions	Channeling	Nitride Voids	Internal Device Shorts	Internal Device Opens
Device Manufacturer	0	2	1	2	0	0	0	0
Device Class	0	1	1	1	3	0	0	0
Device Complexity	0	1	0	0	2	0	3	0
Package Hermeticity	3	0	0	2	0	2	0	0

Key

0 Independence
1 Slightly Dependent
2 Moderately Dependent
3 Highly Dependent

6. ANALYSIS OF DEVICE CHARACTERIZATION DATA

Characterizing beam lead devices according to differences between manufacturers revealed a wide variation in parameters. The overwhelming failure rate and parameter degradation exhibited by linear devices indicate that, unless stringent fabrication and screening controls are imposed, the reliability of such devices is highly suspect.

Beam Hardness – Vendor rank according to beam Hardness is:

Vendor	Hardness
Z	3
Y	2
W	1
X	1

Where 1 is most acceptable (i.e., the softest beams).

Vendor rank by least variation from type to type is:

Z	–	1
W	–	1
X	–	2
Y	–	Not applicable, only one type supplied

Where (1) is least variation.

Beam Peel Strength – Vendor ranking by beam peel strength is:

W	–	1
X	–	2
Y	–	3
Z	–	3

Where (1) is strongest.

Beam Shear Strength – Vendor ranking by beam shear strength is:

Z	–	1
Y	–	2
X	–	2
W	–	3

Where (1) is strongest.

Electrical Parameters – After the devices had gone through all of the screen/stress tests, 20 electrically good devices of each type were randomly selected from the survivors. Electrical test data was taken on each device as detailed in the section on device characterization.

For each parameter of each device type, the mean, standard deviation and t-value (testing significance) was compiled. These data were then compared against the electrical parameters of each device type before being sujected to the screen/stress tests. Results of these tests are given below.

Digital Devices: The surviving digital devices of all types showed very little drift in all major parameters tested. The only notable exception was in the SC 151 (5410) triple 3 input NAND Gate where V_{OH} drifted out of specification on one gate. The drift measured is shown in Table 33 compared to data from Table 8. Out of 47 parameters tested on the 5410, the final device characterization showed a slight drift to an out-of-spec condition on only one parameter.

Even more noteworthy is that out of 217 parameters characterized on the 4 digital types studied, only the one parameter showed a "statistically" significant drift. This seems to indicate that the "good" digital devices are very stable.

Linear Devices: In the linear devices there are significant parameter drifts between initial device characterization and final characterization after the stress tests. Tables 34 through 38 give initial (from Tables 9 to 13) and final readings for all five linear types studied. From these tables it can be seen that all five types of devices were out of specification on one or more parameters after being subjected to the stress tests.

TABLE 33. ELECTRICAL CHARACTERISTICS OF DIGITAL DEVICE SC 151 (5410, NAND GATE)

Test Number	Test Parameter	Spec Value	Pin under Test	Initial Value		Final Value	
				Mean ($\bar{X}$)	STD Deviation	Mean ($\bar{X}$)	STD Deviation
9	V_{OH}	>2.4V	12	2.738	0.031	2.357	0.891

TABLE 34. ELECTRICAL CHARACTERISTICS OF THE SC 152 OPERATIONAL AMPLIFIER (741) FROM VENDOR W BEFORE & AFTER STRESS TESTS

				Before		After	
Specifications			Pin	Measured Value		Measured Value	
Test Number	Test Parameter	Spec Value	Under Test	Mean ($\bar{X}$)	Standard Deviation	Mean $\bar{X}$	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤ 5mv	4.5	-1.708	1.568	-3.636	7.972
2	$\lvert I_{IO} \rvert$	≤ 200nA	4.5	-.871	34.122	-33.803	283.791
3	A_{VOL}	≥ 50K	12	110,478	17,693	114,926	140,537
4	V_{swing}	≥ ±12V	12	13.503	.300	12.056	14.540
5				-12.743	.092	-9.743	4.939

6. ANALYSIS OF DEVICE CHARACTERIZATION DATA (Continued)

TABLE 35. ELECTRICAL CHARACTERISTICS OF THE SC 153 OPERATIONAL AMPLIFIER FROM VENDOR Y BEFORE & AFTER STRESS TESTS

				Before		After	
Specifications			Pin	Measured Value		Measured Value	
Test Number	Test Parameter	Spec Value	Under Test	Mean ($\bar{X}$)	Standard Deviation	Mean $\bar{X}$	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤ 5mv	18,19	.805	2.131	3.180	10.939
2	$\lvert I_{IO} \rvert$	≤ 200nA	18,19	-.270	7.068	25.690	283.387
3	A_{VOL}	≥ 50,000	8	122,068	7,303	84,297	31,131
4	V_{swing}	≥ ±12V	8	13.488	.047	12.943	3.391
5			5	-12.687	.063	-11.680	3.744

TABLE 36. ELECTRICAL CHARACTERISTIC OF THE SC 154 OPERATIONAL AMPLIFIER (741) FROM VENDOR Z BEFORE & AFTER STRESS TESTS

				Before		After	
Specifications			Pin	Measured Value		Measured Value	
Test Number	Test Parameter	Spec Value	Under Test	Mean ($\bar{X}$)	Standard Deviation	Mean $\bar{X}$	Standard Deviation
1	$\lvert V_{IO} \rvert$	≤ 5mv	13,16	1.711	3,239	-.210	18.474
2	$\lvert I_{IO} \rvert$	≤ 200nA	13,16	.065	11.661	-18.295	277.782
3	A_{VOL}	≥ 50,000	3	127,022	8,973	102,601	22,503
4	V_{swing}	≥ ±12V	3	13.283	1.370	11.407	21.582
5	V_{swing}	≥ ±12V	3	-12.200	3.754	-12.839	21.177

TABLE 37. ELECTRICAL CHARACTERISTICS OF THE SC 155 OPERATIONAL AMPLIFIER FROM VENDOR X BEFORE & AFTER STRESS TESTS

				Before		After	
	Specifications		Pin	Measured Value		Measured Value	
Test Number	Test Parameter	Spec Value	Under Test	Mean ($\bar{X}$)	Standard Deviation	Mean $\bar{X}$	Standard Deviation
1	$\|V_{IO}\|$	≤ 5mv	13,16	-2.055	16.126	3.276	11.766
2	$\|I_{IO}\|$	≤ 200nA	13,16	29.981	67.258	383.503	868.088
3	A_{VOL}	≥ 50,000	3	124,311	9,852	123,366	11,476
4	V_{swing}	≥ ±12V	3	12.751	3.789	44.275	225.551
5	V_{swing}	≥ ±12V	3	-13.527	3.891	-17.913	6.520

TABLE 38. ELECTRICAL CHARACTERISTICS OF THE SC 156 VOLTAGE COMPARATOR (710) FROM VENDOR W BEFORE & AFTER STRESS TESTS

				Before		After	
	Specifications		Pin	Measured Value		Measured Value	
Test Number	Test Parameter	Spec Value	Under Test	Mean ($\bar{X}$)	Standard Deviation	Mean $\bar{X}$	Standard Deviation
1	$\|V_{IO}\|$	≤ 2mv	2,3	.445	.928	5.821	24.847
2	$\|I_{IO}\|$	≤ 5μA	2,3	-.277	.902	134.105	971.409
3	A_{VOL}	>1250	7	72,845	70,398	77,243	26,996
4	V_{OH}	2.5-4.0V	7	2.880	.146	1.773	3.165
5	V_{OL}	-1.0-0.0V	7	-.191	.240	0.336	2.752

Section 2 – Beam Lead Reliability Study
Subsection D – Recommendations

1. RECOMMENDED SCREENING FOR BEAM LEAD DEVICES

Five specific screening tests are recommended to ensure that vendors of beam lead devices provide reliable devices in the most economical way. These screens will minimize the failure modes uncovered by this study, regardless of the cause of failure.

In order to recommend adequate techniques for minimizing failures in future beam lead devices, it is first necessary to review the failure mechanisms.

The cause of the beam lead device failures that were found during the course of the study can generally be categorized as follows:

- Environment Induced Failures – Those caused by moisture and saline solution.
- Beam Lead Process Related Failures:
  - Nitride Voids
  - Interconnect Delamination
  - Spalling Gold
  - Interconnect Shorts
- Those caused by variations from targetted to actual material thicknesses and composition (see device characterization Table 16).
- Workmanship Related Failures:
  - Pattern Misalignment
  - Photoresist Breakdown
- Standard Semiconductor Failures:
  - Infant Mortality
  - Internal Opens and Shorts
  - Channeling
- Design Failures:
  - Hot Spots on the Dice

Appropriate screening by the vendors is recommended as the best means for minimizing the effect of all of the above causes. The basic purpose behind the screens recommended is to provide beam lead devices from the vendor to the user which ensure both (1) high yield, and (2) high reliability in the hybrid circuits fabricated with the beam lead devices.

As many of the screens as practical should be of the batch process type, and which (for the sake of economy) are done at either the lot level or the wafer level.

At present, all major beam lead manufacturers, have or are developing individual beam lead device carriers which allows for the power testing and screening of beam lead devices on an individual basis such as is done with conventional JAN-TX type semiconductors. Where power screens are recommended it assumes that the beam lead devices will be in the individual carriers. No moisture screening is recommended because the study results indicate that devices under power in a moist environment (even when conformally coated or molded) will fail either due to gold migration or moisture-induced shorts between adjacent interconnect when the devices are powered. The recommended screens will be on five levels:

1. Vendor process qualification-oriented screens, which ensure that the vendor processes result in beam lead material layers of specified thickness and composition.

2. Vendor design qualification to ensure that devices are thermally acceptable.
3. Vendor process control checks to ensure that beam lead devices are consistently reliable from process run to process run.
4. Screens to ensure a high level of vendor workmanship.
5. Screens to weed out infant mortality.

The screens are described in detail below.

In addition to these recommended screens, it is also recommended that devices be accepted or rejected on a lot basis. At this level the minimum yields for each screen must be established. Lots are to be accepted only if the entire lot meets the minimum-specified yield for each screen. This ensures good quality devices, free from defects that may be inherent in that particular lot.

RECOMMENDED VENDOR QUALIFICATION SCREENS
FOR BEAM LEAD DEVICES

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1. Process Qualification Screen: Vendor to supply:

   a. SEM photos at applicable high magnifications and SEM microprobe data on each device type to ensure proper oxide, silicon nitride, platinum silicide, titanium, platinum, and gold thickness and composition.
   b. Beam hardness data for each device type
   c. Beam peel and shear strength data for each device type

   Here definite material specifications must be established by joint committee and subsequently imposed by MIL-SPEC upon the beam lead manufacturers. Frequency: data must be provided one time to qualify each vendor, and then each time a new device type is released.

2. Thermal Qualification Screen: Vendor to supply thermal maps on each device to ensure that dice contains no hot spots. Frequency: data must be provided with each new device type or when there is a change in device interconnect pattern.

3. Process Control Screen: Vendor to supply the same data as in screen (1) above. Frequency: data must be provided to purchaser with each different vendor processing lot.

4. Workmanship Screen: Vendor to conduct screening at the wafer level as follows:
   a. Front side visual inspection at 100X minimum (100%)
   b. Back side visual inspection at 100X minimum (100%)
   c. Sodium ion penetration test (sample only)
   d. DC probe (100%)

5. Infant Mortality Screen: Vendor to conduct 100 percent screening at the dice level as follows:

   a. Age bake, 72 hours at 300°C (MIL-STD-883, Method 1008, Condition F)
   b. AC test key parameters, using beam lead carrier
   c. High temperature reverse bias, 168 hours at 150°C (MIL-STD-883, Method 1005)

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SECTION 3
BOND INTEGRITY STUDY

1. VARIABILITY OF BEAM BONDING PARAMETERS

Beam lead bonding parameters (bonding force, temperature, push-off strength) were measured to determine the acceptable beam-to-substrate bondability conditions (high strength and low resistance) for each device type. The pressure settings of the bonding machine, determined by trial and error, were selected to ensure uniformity of the data.

Section 2 described how nine different types of beam lead devices were selected for use in the study. Before the modules could be fabricated for the Stress/Screening tests, it was necessary to determine the settings of the beam lead bonding machine (the bonder used was a K&S 576 Beam Lead Wobble Bonder) that would give both acceptable beam-to-substrate conductor bond strength and low beam-to-conductor contact resistance. Ball-park bonder settings were recommended by the bonder manufacturer. Final settings for each device type were determined by trial and error. For a given device type several devices would be bonded, then bonds were visually examined for deformation, squash out, and bond length, as shown in Figure 73. Push-off tests were then made and push-off strengths recorded. Two grams per beam was set as the lower acceptance limit for bond strength. Then, as required, machine settings were changed and the process was repeated until settings were determined for each device type that assured that the bonds met the minimum acceptable visual, bond strength, and contact resistance requirements.

Early in the study it was decided that all devices should see the same time-temperature conditions during all phases of the study so that screen/stress test data for each device type could be evaluated on a one-for-one basis. Thus the bonding collet temperature and the substrate temperature had to be high enough to accommodate each different device type. Once determined, these were held constant, along with bond time, for each device type and bonding force was varied to provide for beam material variations from device type to device type.

Beam lead bonding parameters and bond strength data for each device type is given in Table 39. From Table 39 is seen that each different device type required a different bonding force. This primarily means that beam lead hybrid manufacturers have two options: (1) bond each different device type on a different wobble bonder, or (2) reset the machine each time a new device type is bonded.

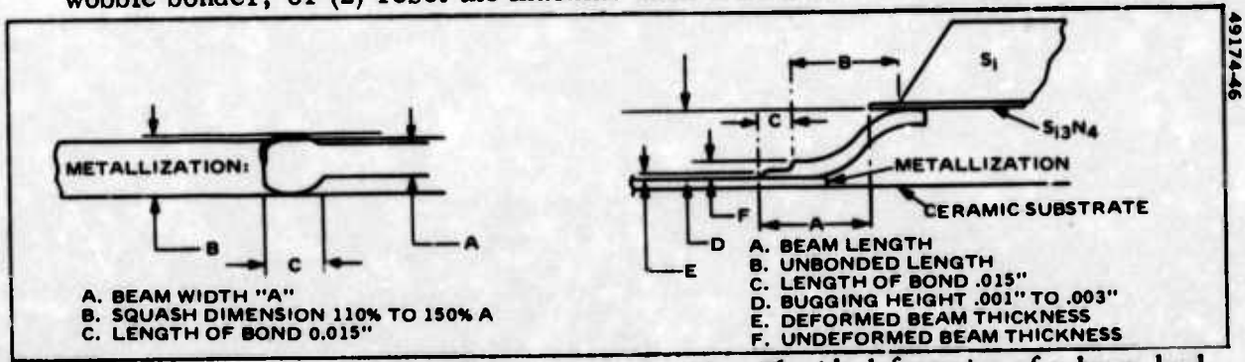

Figure 73. Beam Lead Bond Visual Acceptance Criteria. The ideal footprint of a beam lead device bonded to a conductor or substrate is indicated principally by dimensions C and E. The size and shape of this footprint determines the physical and electrical characteristics of the bond.

TABLE 39. BEAM LEAD BONDING PARAMETERS AND BOND STRENGTH DATA

Device Code/ Type	Mfg	No. of Beams	Beam Hardness (Knoop No.)	Beam Thickness	Bonding Force (grams)	Push-off Strength (grams)	Average Push-off Strength (grams/beam)
SC148 Digital 5473	W	24	42	0.66	300	56	2.3
SC149 Digital RF100	X	16	53	0.60	225	43	2.7
SC150 Digital 5400	W	14	60	0.71	200	36	2.6
SC151 Digital 5410	Z	14	63	0.49	200	36	2.6
SC152 Linear 741	W	18	39	0.33	240	37	2.0
SC153 Linear 741	Y	10	54	0.51	150	27	2.7
SC154 Linear 741	Z	20	64	0.47	250	45	2.3
SC155 Linear RM101	X	20	39	0.50	250	44	2.2
SC156 Linear 710	W	12	46	0.63	150	31	2.6

Bonding Collet Temperature - 380°C

Substrate Temperature - 300°C

Dwell Time - 2 seconds

Revolutions - Two

2. MODULE FABRICATION AND TEST PROCEDURE

The purpose of this part of the program was to evaluate lead bond integrity resulting from the removal and replacement of beam lead devices on thick or thin film substrates. The program was divided into three tasks: device replacement, beam lead rework, and detailed tests and data evaluation.

Dice replacement or repair is a normal operating mode in the fabrication of hybrid modules. It is therefore necessary to understand how the repair of bonds, individually and collectively, at a given site affects beam lead reliability. Since device replacement involves the repetitive removal and rebonding of all beam leads at one time, a special procedure was established to ensure uniformity of the data obtained over the different device cycling steps. Figure 74 (following) diagrams the details of the replacement task, and Figure 75 (following) illustrates how this task fits into the overall bond integrity evaluation procedure. In addition to the replacement task, a rework task was conducted to evaluate the effects of reworking individual beam-to-substrate bonds at one dice site. These tasks were done using both thick and thin film conductors.

Replacement Task Preparation Using Thick Films — The thick film modules were fabricated similar to those detailed in the Section 2 topic "Hermetic and Non Hermetic Device Fabrication." Here a thick film conductor pattern was printed with Cermalloy 4300 B fine line gold on 96% alumina T08 substrate and fired. After firing, to provide for the push-off tests, a 0.018-inch diameter hole was drilled in the center of the substrate.

Replacement Task Preparation Using Thin Films — For the thin film modules, the 96% alumina T08 substrates were metallized with sputtered nichrome, and in the same sputtering cycle a layer of gold was deposited. After sputtering additional, gold was plated over the sputtered gold to provide for low conductor resistivity and good device bondability. After plating, the device conductor pattern was delineated using conventional photomasking and etching techniques. Then as with the thick film substrates, a 0.018-inch diameter hole was drilled in the center of the substrate to provide for the device push-off tests.

Device Bonding and Testing — Devices were next attached to both the thick and the thin film substrates by wobble bonding with a Kulicke and Soffa Model 576-1 Beam Lead Wobble Bonder. After wobble bonding the devices, the substrate was placed over a T08 header and thermocompression gold wire bonds were made between each substrate conductor pad and the corresponding pin on the header. In this way, after electrical testing and screening the substrate could be removed from the header to perform the push-off test. (The beam lead device type used for the push off tests was the 710 voltage comparator from vendor W.)

Electrical testing was done at key points during the task. At these points, the following parameters were measured on a go/no go basis: V_{off}, V_{OH}, V_{OL}. After Electrical test, the substrates with the beam lead device were visually inspected, they were then removed from the headers, and push-off tests were done. The push off-force was recorded along with data such as number of beams

broken, where the break occurred, extent of damage to substrate conductor pattern, and any other pertinent anomalies. After each push-off cycle, the conductor pads had to be "cleaned up" for the next device bonding cycle. For the clean-up, all substrate conductor pads were visually inspected, residual beam metal was removed with tweezers, and the beam-to-conductor bonding areas were manually flattened with a stainless steel tool.

Conduct of the Rework Task — A separate task, the beam lead rework task, was done in order to evaluate the effect of reworking or repairing one or more beams on a given beam lead device rather than replacing the entire device. Two methods were investigated to repair the beam. In one case, each beam lead device went through the entire bonding cycle again. In the other case the loose bonds on a given device were individually reworked by thermo-compression wedge bonding that particular beam.

In order to produce chips with misbonded leads, the beam lead wobble tool was adjusted so as to be out-of-parallel with the substrate. A series of 10 devices were bonded with the equipment adjusted in this manner. This resulted in beam lead modules where the devices had one or more beams not bonded to the substrate. The 10 circuits were divided into two groups of 5 each for the two methods of rework: (1) Re-wobble bond entire device, and (2) TC bond individual beams.

Test and Evaluation Tasks — After completion of the fabrication, replacement, and rework work cycles the modules were routed to visual inspection, electrical test and environmental test. Here the modules were subjected to the same basic stresses as class B hybrids in the effort to determine how the repeated device replacement and rework would effect a hybrid module similarly built. The flow of the modules through the environmental tests is detailed in Figure 75.

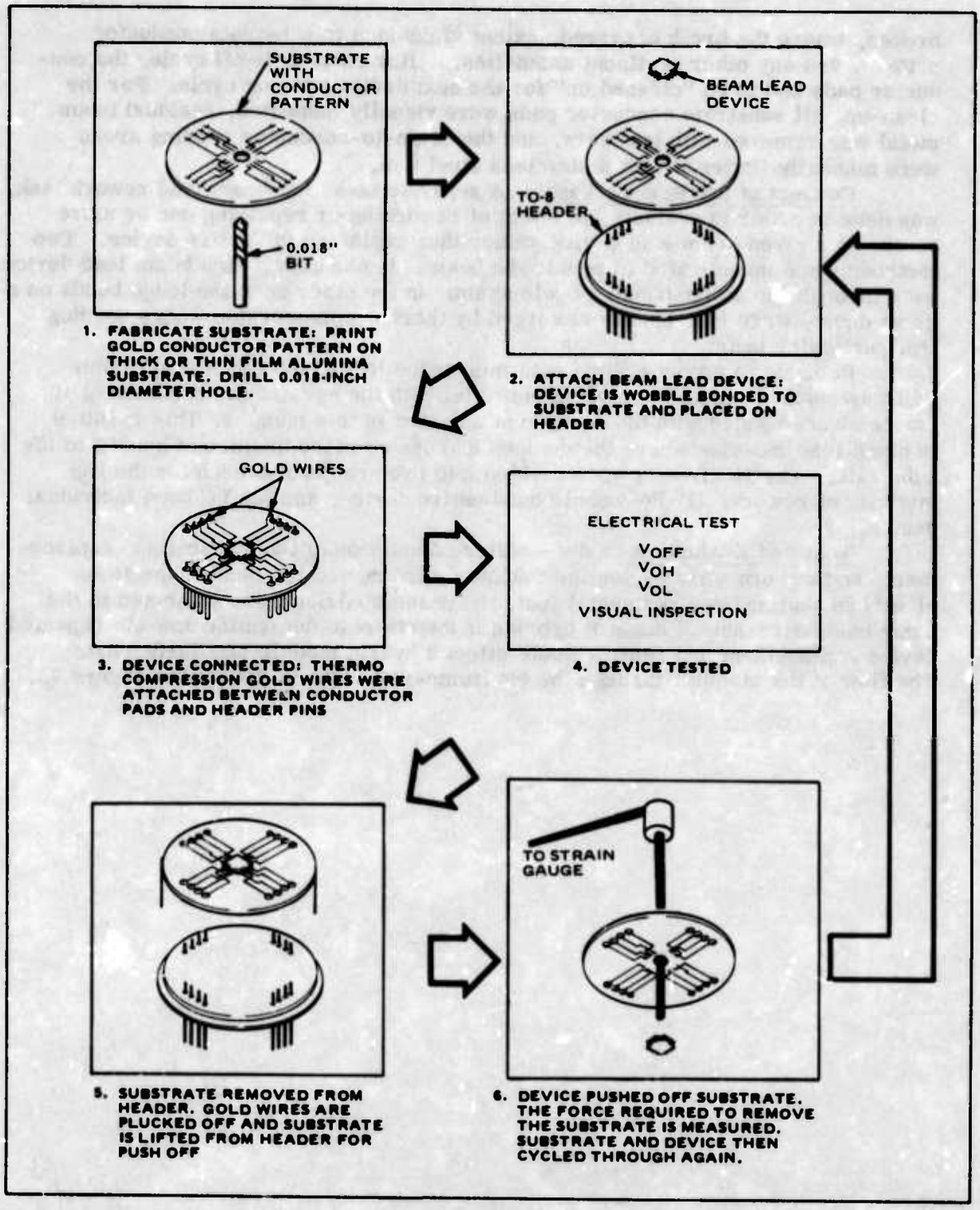

Figure 74. Fabrication and Replacement Steps for Conducting the Bond Integrity Study. Each die was recycled 10 times for the replacement study.

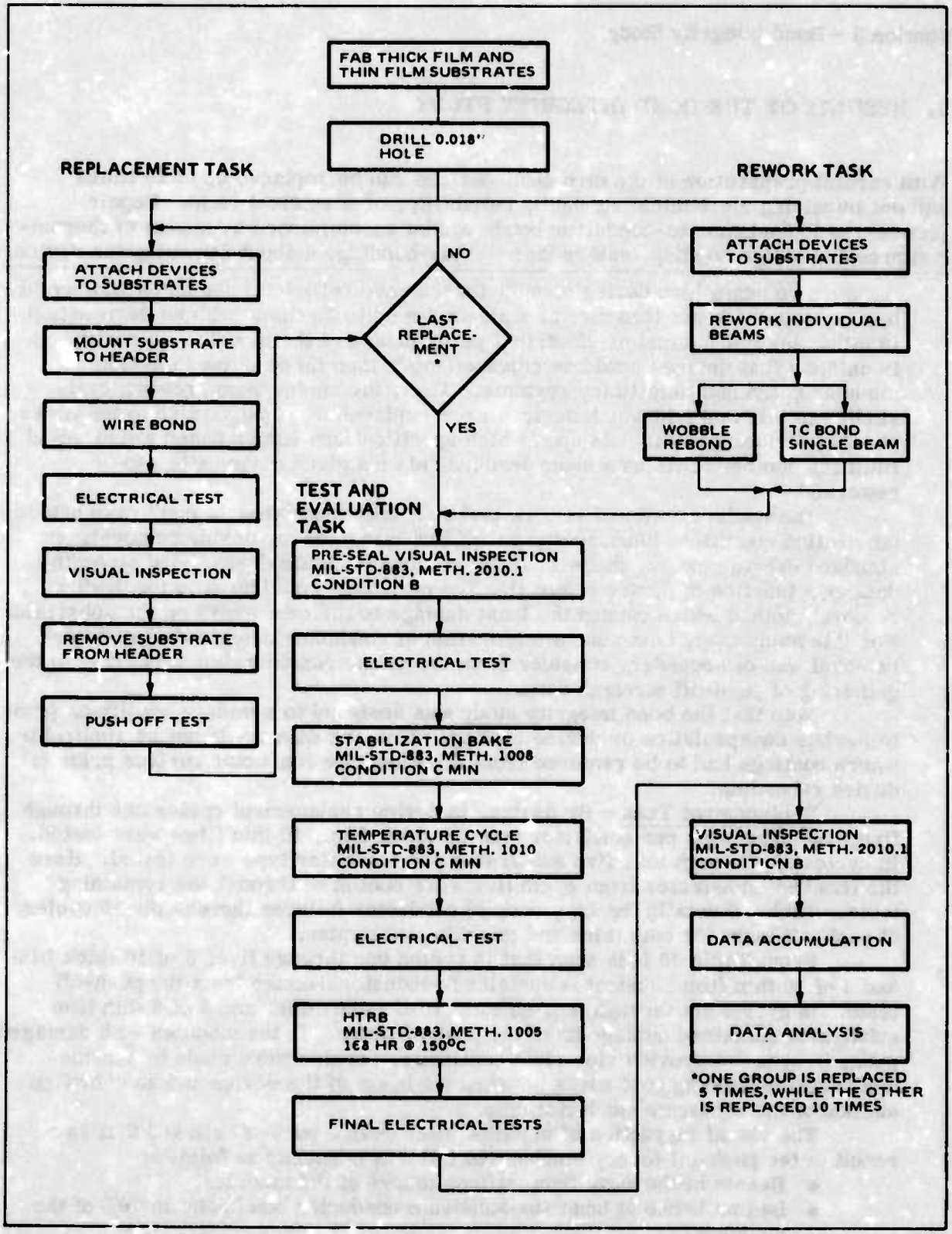

Figure 75. Flow of Bond Integrity Evaluation. The replacement and rework portions of this study were conducted in parallel prior to common environmental and electrical tests.

3. RESULTS OF THE BOND INTEGRITY STUDY

With careful preparation of the dice site, devices can be replaced up to 10 times without impairing mechanical strength, reliability, or electrical yield. Repair (rework) of loose beam-to-conductor bonds can be accomplished by means of thermocompression wedge bonding, rather than wobble-bonding, without damaging the device.

Two beam lead device manufacturers have reportedly (on an experimental basis) replaced beam lead dice at a given site up to 25 times with no degradation in either the mechanical or electrical performance of the module. In reality, it is unlikely that devices would be replaced more than three times in hybrid modules delivered to military systems. Thus, the replacement/rework cycle studies in this task, in which devices were replaced or repaired five to ten times, should provide realistic data upon which specifications can be based which would limit the number of times a beam lead hybrid or a given device site can be reworked.

The replacement and rework tasks actually simulated "worst" case hybrid fabrication conditions because a push-off test was used for device removal. In standard hybrid rework, there would be no need to obtain device bond strength data as a function of device removal. The emphasis would be upon the device removal method which caused the least damage to the conductors on the substrate. For this study task, however, minimization of conductor damage during device removal was of secondary consideration; the prime consideration was given to the gathering of push-off strength data.

Note that the bond integrity study was designed to simulate conditions prior to module encapsulation or device coating. Thus the data would not be applicable where coatings had to be removed from the substrate conductor surface prior to device rebonding.

Replacement Task – By design, in device replacement cycles one through five, ten substrates per conductor type (10 thick film, 10 thin film) were tested. In cycles six through ten, five substrates per conductor type were tested. Here the five best substrates from cycle five were continued through the remaining tests. Table 40 details the frequency of conductor failures through the 10 cycles of push-off tests for both thick and thin film substrates.

From Table 40 it is seen that in cycles one through five, 3 of 10 thick film and 4 of 10 thin film substrates sustained conductor damage from the push-off tests. In cycles six through ten, no thick film substrates, and 2 of 5 thin film substrates sustained damage from the push off tests. In the modules with damaged pads, in order to provide electrical continuity, repairs were made by thermocompression bonding gold wires between the beam of the device and an unbroken section of the substrate conductor line.

The visual inspection of modules after device push-off showed that as a result of the push-off force, mechanical failures occurred as follows:

- Beams broke away from silicon in 25% of the modules.
- Beams broke at beam-to-substrate conductor bond point in 70% of the modules.
- Conductors pulled away from substrate in 5% of the modules.

The push-off strength data for both thick film and thin film substrate is given in Figure 76. The average push-off strength is based on 12 beams/device being bonded to the substrates. Substrates with any defective conductor pads are not included in the averages.

It is seen that for thin film conductors, the average push-off strength ranges between 24 and 40 grams while the range for thick film conductors is 31 to 36 grams. The minimum acceptable push-off strength level given by several beam lead hybrid suppliers questioned was 2 grams/beam. Thus, for the replacement task, where the 710 comparator with 12 beam was used, the minimum acceptable push-off would have been 24 grams. Only on the third thin film cycle (upper curve of Figure 76) was this lower acceptance level reached.

Figure 77 shows the effect of repeated device replacement at a given site upon the electrical yield of the new devices bonded to the reworked substrate conductor sites. Of significance is the fact that the yield is relatively stable throughout the ten cycles for both thick and thin film. If the contact resistance of the conductors was increasing due to deterioration of the substrate conductor metallurgy, the trend should be one of increased electrical rejection with increasing replacement cycle. This is not the case, indicating that device replacement through up to 10 cycles will not adversely effect the electrical yield of the modules.

After the push off tests from the tenth device replacement cycle were completed, the substrates were inspected. Because three of the thin film substrates were already damaged, all thin films were discontinued from further tests. In the case of the five thick film substrates, devices were wobble bonded to the substrates. The substrates were then re-attached to the headers and the devices were tested. Four of the five devices were functionally good, and were routed to environmental tests after HTRB the four devices were electrically tested. Two of the four devices were failures. This, however, is in line with the failure incidence reported in the reliability study, and thus the failures were not attributed to the reiterative replacement.

TABLE 40. NUMBER OF SUBSTRATE CONDUCTOR FAILURES AS A FUNCTION OF DEVICE REPLACEMENT CYCLES

Devices/ Conductor Type Under Test	Number of Test Cycles	Cumulative Total Pads Lost		Cumulative Total Substrates Partially Defective		Cumulative Total Substrates Discontinued From Further Tests	
		Thick Film	Thin Film	Thick Film	Thin Film	Thick Film	Thin Film
10	1	0	0	0	0	0	0
	2	2	8	2	4	0	1
	3	0	0	0	0	0	0
	4	0	10	0	0	0	0
	5	4	0	3	0	0	0
5	6	0	1	0	1	0	0
	7	0	2	0	2	0	0
	8	0	3	0	2	0	0
	9	0	0	0	0	0	0
	10	0	0	0	0	0	0

Device Under Test: Class, Linear; Type 710; Function, Voltage Comparator; Vendor, B; Number of beams, 12.

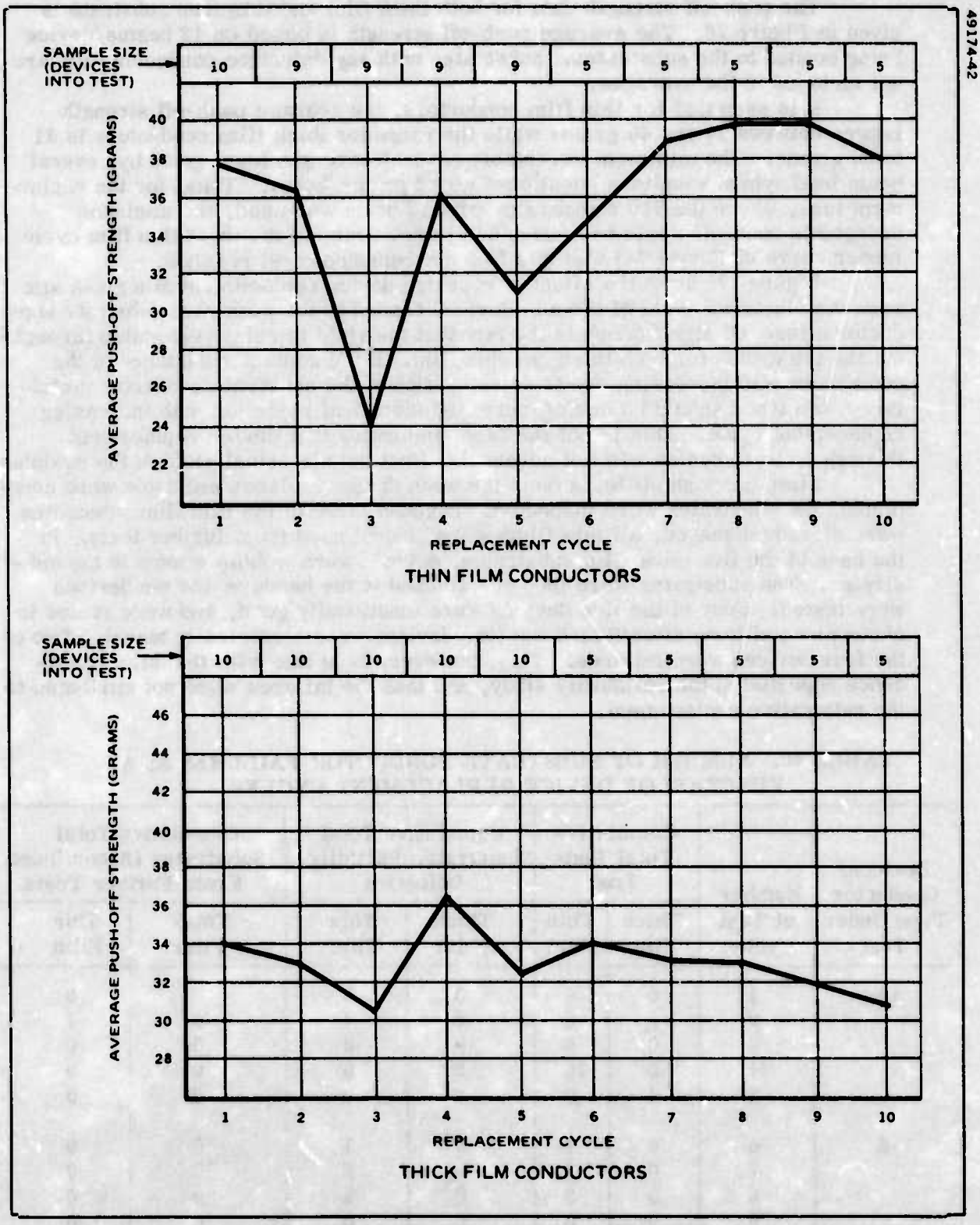

Figure 76. Device Push-Off Strength as a Function of Number of Times Repeated

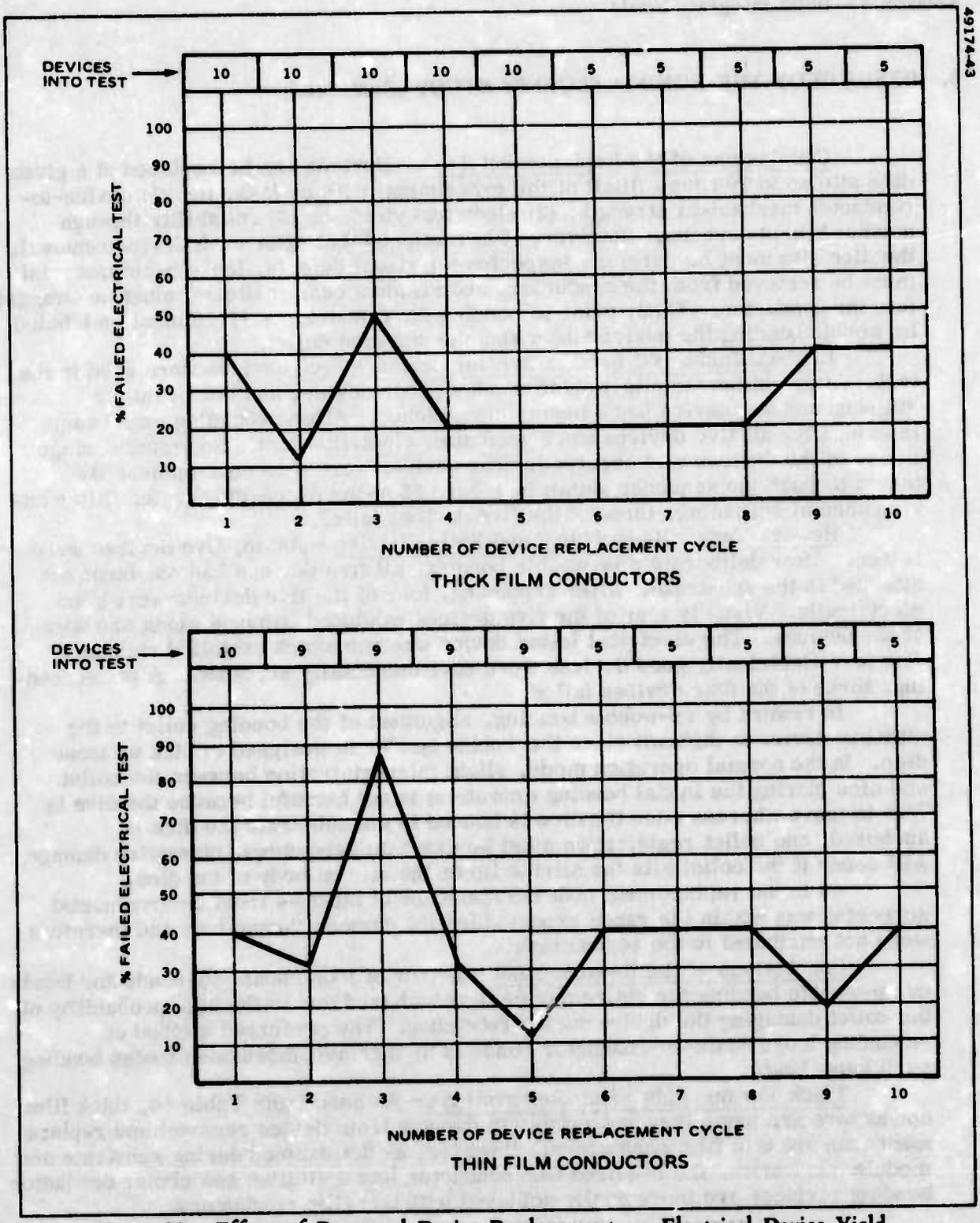

Figure 77. Effect of Repeated Device Replacement on Electrical Device Yield

3. RESULTS OF THE BOND INTEGRITY STUDY (Continued)

Conclusions of the Replacement Task – Devices can be replaced at a given dice site up to 10 times (limit of the experiment) with no loss, in: (1) device-to-conductor mechanical strength, (2) electrical yield, or (3) reliability through normal hybrid screens. However, it is cautioned that after each device removal, the dice site must be carefully inspected for visual defects, loose beam material must be removed from the conductor, and residual beam material must be swagged into the conductor. Then, prior to bonding the conductor surface must be labeled by wobble bonding the device site with an empty dice collet.

Rework Task: TC Bond Individual Beams – Five devices were used in the test. After deliberate mis-wobble bonding, four devices had one beam not attached and one device had 3 beams not attached. After rebonding each beam individually, all five devices were good after electrical test. No visual damage to any of the devices was observed. The devices were then environmentally tested through the sequence shown in Figure 75 of the preceeding topic. After environmental screening, three of the five devices failed.

Rework Task: Re-wobble Bond Entire Device – Again, five devices were tested. After deliberate mis-wobble bonding, all five devices had one beam not attached to the substrate. After rebonding, four of the five devices were good electrically. Visually four of the five devices exhibited chipping along one edge of the devices. The electrical failed device was one which exhibited chipping. The four electrically good devices were environmentally screened. After screening, three of the four devices failed.

In rework by re-wobble bonding, alignment of the bonding collet to the attached device is difficult since the wobble bonder is designed to pick up loose dice. In the normal operation mode, slight misregistration between the collet and dice (during the initial bonding operation) is not harmful because the dice is free to move whereas once the dice is bonded to the substrate the dice is anchored, and collet registration must be exact (to rebonding), otherwise damage will occur if the collet hits the nitride lip or the silicon body of the dice.

As in the replacement task the incidence of failures from environmental screening was within the range expected for the devices themselves and therefore were not attributed to the rebond task.

Conclusions of the Rework Task – Repair of loose beam-to-conductor bonds by re-wobble bonding the entire device is not advised due to the high probability of the collet damaging the device during rebonding. The preferred method of rebonding loose beam-to-conductor bonds is by thermocompression wedge bonding each loose beam.

Thick Versus Thin Film Observations – As seen from Table 40, thick film conductors are much less susceptible to damage from device removal and replacement than are thin film conductors. However, as determined during substrate and module fabrication, the required fine conductor line definition and planar conductor bonding surfaces are more easily achieved with thin film conductors.

SECTION 4
CONCLUSIONS

Section 4 – Conclusions

1. ASSESSMENT OF BEAM LEAD RELIABILITY

The improvements in reliability and cost to be achieved by the use of beam lead devices, as promised in 1972, are compared with the findings of this study. In general, the study shows that beam lead devices do not live up to their promise.

The Promise – As was stated in the introduction, the promise of increased reliability and decreased cost led the military to commit itself to increased use of beam lead devices in future contracts. Promises of improvements in reliability resulted from claims that the metallurgy was less prone to migration, that the silicon-nitride sealed junctions were impervious to sodium-ion contamination, and that the integral beams would eliminate wire bond failures. The claims for reducing cost were: the reduced assembly times would enable bonding to be accomplished in a fraction of the chip-and-wire bonding cost; the ability to completely AC test the device before the hybrid assembly step would reduce rework; and that the beam lead device would operate reliably with a simple polymer coating, thereby eliminating the need for hermetic packaging.

Additionally, it was felt that further cost savings could be realized over the life cycle of a system through the use of beam lead devices. Here, by virtue of the then-reported lower failure rate of beam lead devices in comparison to standard semiconductor devices (0.005%/1000 hours failure rate for beam lead devices), it was anticipated that systems repairs would be fewer and less frequent.

Study Conclusions – The essential findings of this study are listed on the facing page. The overriding conclusion is that beam lead devices do not satisfy the promises cited above. First, beam lead devices may not operate reliably in non-hermetic environments when protected by plastic coatings. During the study, 100% of all devices sealed with water or salt water failed. For the plastic sealed devices subjected to "wet" screens (biased moisture life, boiling water, salt atmosphere), 55.6% of the devices failed in comparison to 19% of those sealed hermetically in dry nitrogen.

Second, beam lead devices were developed to eliminate or reduce many failure modes prevalent in standard semiconductors, such as ionic contamination, interconnect corrosion, lead bond failures, etc.; however, since beam lead devices are more complex and require more processing steps to produce, they have actually opened up failure modes that do not exist in the majority of standard semiconductors. These "unique" beam lead device failure modes include; (a) poor adhesion between interconnect metal and the device, (b) nitride voids, (c) high incidence of channeling due to the number and complexity of device dielectric layers, and (d) delamination of interconnect metal during thermal stress. Thus, beam lead devices in solving one group of problems, have introduced new problems.

Third, beam lead devices are presently not cost effective. Simply, a beam lead device cost 2 to 3 times more than an equivalent semiconductor chip. The low hybrid module rework rate promised through the use of beam lead devices (except at the expense of extensive, costly device pre-screening) is not a reality as evidenced by the high incidence of device failures from first electrical test through the screens/stress tests as shown in Tables 23 through 29.

Fourth, there apparently is no standard beam lead process as evidenced by the data in Table 16. Here wide variations in key material layer thickness exist not only from vendor to vendor but between vendor target and vendor actual values.

Fifth, linear beam lead devices are extremely failure prone. The linear devices failed at a 2:1 rate over digital devices (see Table 26). The higher incidence of linear failures is most probably due to their higher operating voltage and/or to their greater susceptibility to channeling.

Sixth, at present, there is no standardization from vendor to vendor for a given device type. In the study, all four operational amplifiers (from the four different vendors) were different in size, number of beams, and pin-in and pin-out. Thus, each vendor's operational amplifier required separate substrate layouts. This essentially means that once a hybrid is designed with beam lead devices from a given vendor, that device is for all practical purposes a "sole source" item.

Seventh, reliability and failure rate data for beam lead devices currently quoted must be re-evaluated. It is obvious from the data in Tables 23 through 29 that the failure rate of beam lead devices is considerably in excess of the 0.005%/1000 hours expected at the beginning of the study.

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Appendix A
VENDOR BEAM LEAD SCREENING PROCEDURE

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Appendix A

VENDOR BEAM LEAD SCREENING PROCEDURE

In order to assess the true impact of the failure data obtained from the study, and consequently to recommend valid screening procedures, it was necessary to determine how good (or bad) were the devices supplied by the different vendors for the study. Two members of the study team interrogated each vendor to establish the screens and level of screens performed against each device purchased according to the purchase order number. In the case of vendors W, X, & Z, a trip was made to each of the suppliers plants and discussions were held. In the case of vendor Y, telephone conversations were used to gather the data. The screens to which devices were subjected prior to their use in the study are shown in Table A-1.

From Table A-1 (and with reference to the study results), the following points are noted:

(1) Vendor X, who did more screening than the other three vendors, had a somewhat lower failure incidence through the screens/stress tests.

(2) There is no standardization in screening from vendor to vendor.

(3) The screens used were ineffective in eliminating potential device failures.

TABLE A-1. VENDOR BEAM LEAD SCREENS USED ON THE DEVICES SUPPLIED TO THE RELIABILITY STUDY

Purpose	Vendor W	Vendor X	Vendor Y	Vendor Z
Nitride Efficiency	Sodium ion penetration test	Sodium ion penetration test	Nitride etch rate test	Nitride etch rate test
Interconnect Adhesion Test		Interconnect scratch test		
DC Electrical Parameter Verification	DC Probe (100 %)	DC Probe (100%)	DC Probe (100%)	DC Probe (100 %)
AC Electrical Parameter Verification		Sample AC Test		
QA Verification of Production Test		QA DC Probe (LTPD 10%)		QA DC Probe (LTPD 10%)
Workmanship Verification	Backside Visual (20%)	Backside Visual (1% AQL)	Backside Visual (sample only)	Backside Visual (100%)
	Front side visual (20%)	Front side visual (100%)	Front side visual (sample only)	
QA Verification of Production Test	QA Backside visual (LTPD 15%)	QA Backside visual		QA Backside visual (LTPD 15%)
		QA Frontside visual		
Beam Adhesion Test	Dice pushoff test (PDA 10%)	Dice pushoff test (20 units/wafer)	Dice pushoff test (10 units; accept on 1, reject on 2)	Dice pushoff test (PDA 10%)

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Printed by
United States Air Force
Hanscom AFB, Mass. 01731